1-1-2001

Characterization of 1/f noise in bird's beaking region of MOS transistor

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Characterization of 1/f noise in bird's beaking region of MOS transistor

By

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A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:
Dr. Randall Geiger (Major Professor)
Dr. Chris Chu
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Dr. Jim Hellums

Iowa State University

Ames, Iowa

2001

Graduate College
Iowa State University

This is to certify that Master's thesis of

Paras Dagli

has met the thesis requirements of Iowa State University

Signatures have been redacted for privacy

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ACKNOWLEDGEMENTS

There are many people whom I would like to acknowledge for their assistance and support in completing this work, both technical support and advice as well as moral support. Words can little express my gratitude towards my advisor, Professor Randall Geiger, for his guidance and insight, and also for his patience in seeing this work through. It has been a great privilege to be in his research group, and undoubtedly the credibility and prestige of his name will continue to open doors for me in the future.

I'd also like to express my special gratitude towards outside committee member Dr. Jim Hellums, TI Fellow, from Texas Instruments, Inc. Being the 'guru' in the noise field, coupled with his many years of design experience, has allowed him to focus in on the critical and interesting issues of any problem. I was truly very fortunate to have the opportunity to work under his mentorship throughout the course of this thesis. Fabrication of silicon is always a complicated problem. Jim Hellums deserves special thanks for all the work he did to help get my test structures fabricated at Texas Instruments, Inc. Other people at TI I'd also like to thank for their fab help are Baher Haroon, Doug Goodpaster, Grant Miller, Dave Jaska. I'd also like to thank numerous other people at TI and to name a few Keith Green (for access to noise measurement system and support), Don Ladwig, Tarry Machost (technicians), Praful Madhani, Jeff Wu (technical discussions), Wayne Chen(my current supervisor), Ron Cox, Paul Ehnis etc.

I can not finish this note without mentioning some key people at ISU who helped me finish this thesis. I am thankful to my other committee members Dr. Tim Stahley and Dr. Chris Chu for taking time to read my thesis and making helpful suggestions. I am also

thankful to Dr. Edward Lee and Dr. Bill Black for helpful discussions during the course of thesis. Finally, I would like to thank some of my day in day out buddies in my office space at ISU. Mark Schlarman has been a great friend for all the technical as well as non technical discussions. Some of his MS word related tips and templates has saved me awful lot of time. Saqib Malik has always been available for all the technical and other issues. I'd also like to thank my other colleagues Yonghui Tang, Yonghua Cong, Mao Feng Lan, Srikanth Gondi, Kumar Parthasarathy, Jing Ye and many other graduate students at ISU.

Next, I'd like also to thank Texas Instruments, Inc. for their financial support through the graduate research assistantship program.

Last, but certainly not the least, I'd like to thank my parents for their unyielding love and encouragement. I admire their sacrifices and I'd like to dedicate this accomplishment to them.

Paras Dagli

CHAPTER 1

INTRODUCTION

1.1 Motivation and goal

To develop good analog circuit design techniques, a basic understanding of noise sources and analysis is required. Noise calculations are often assumed to be 'black magic' affairs, and circuit optimization assumed to be even blacker. Noise can interfere with weak signals when the transistor is part of an analog circuit, so ways to predict and possibly reduce noise are important. For this reason, the subject of noise in MOS transistors has received extensive treatment in the literature. IC designers have experienced a lack of adequate simulation models for predicting noise in MOSFETs when they try to meet a tight specification in terms of dynamic range.

Recently the flicker noise characteristics of MOSFETs are receiving increasing levels of attention due to the widespread application of MOSFETs in the area of precision analog integrated circuits. The capability of integrating low noise analog circuits and high speed digital circuits on the same chip is crucial to the production of high performance MOS integrated circuits such as A/D converters and communication circuits. Compared with bipolar transistors, MOS transistors offer some unique features, such as high input resistance, low area and low power dissipation. On the other hand, MOS transistors tend to generate more noise than their bipolar counterparts, especially in the low frequency region where the flicker noise dominates. Low frequency noise (Flicker noise or 1/f noise) dominates the noise performance of most MOS amplifiers below a few kilohertz and often is the dominant noise source even at much higher frequencies.

The understanding of low frequency noise, or 1/f noise, has been a difficult challenge and many areas of its origin and behavior are still not understood. Although many investigations have been performed focusing on modeling the 1/f noise in MOS transistors, no definitive theory has been set forth to accurately explain the diverse results observed with real devices in the laboratories. Universally accepted model explaining the 1/f noise in all p- and n-channel MOS transistors is still lacking. Mathematical form of current spectral density (S_{if}) of all popular models is not compatible with small signal models. There is also (nontrivial) parameter confusion among the design community for flicker noise co-efficient (K_f) since there is no unique model. Hence, it is possible to have different values and units of K_f from one vendor to another.

As the device dimensions continue to shrink with each new generation of MOS technology, the effect of an individual defect on device performance becomes more pronounced. Bird's beaking may be one of them. During the field oxide growth, encroachment into the active region effectively reduces the width of the transistor, which is called bird's beaking. For short channel devices, bird's beaking could be a significant part of overall width of a transistor. In the past, most of the work on 1/f noise in MOSFETs published in the literature had focused on the effects of oxide traps near the interface, but no attention had been paid to the area of bird's beaking(side wall noise effects). Our conjecture is that 1/f noise is worse in bird's region of MOS transistor. We will evaluate 1/f noise performance of MOS transistor with and without bird's beaking. Particular emphasis will be focused on determining how K_f(flicker noise co-efficient) for the birds beaking region compares with that for the other region.

Typically, designers utilize the rectangular-shaped gate whenever possible since the rectangular geometry is convenient for layout, component density can be high and good models for this device have been developed. Nonrectangular devices (e.g. trapezoidal, toroidal, circular, 'V' shaped etc.) are occasionally used, however. We will evaluate flicker noise performance of nonrectangular transistors without bird's beaking and determine if geometry of the device affects the noise performance. If geometry of the device as well as elimination of bird's beaking helps to reduce noise in the device, improvements in performance can be obtained by using these structures.

1.2 Thesis organization

In chapter 2, noise modeling fundamentals are covered. It includes some basic noise terminology such as different types of noise, noise sources, noise measures, etc and describes the consistency problem in detail. It covers the consistency problem for both series and parallel connected devices.

In chapter 3, background on 1/f noise is given in detail. It includes some general 1/f noise observations and describes physical mechanisms governing 1/f noise - both number fluctuation and mobility fluctuation models - in detail. Overview and assessment of existing models are covered as well.

Chapter 4 covers the flicker noise characterization and management issues. It describes the flicker noise dependencies in detail and explains our main hypothesis of bird's beaking in rectangular and non-rectangular structures. Inconsistency in existing models is shown with some HSPICE simulations.

Noise measurement is described exhaustively in Chapter 5. Basic setup of our measurement and measurement procedure is described in this chapter. Based on our experience some general guidelines to reduce ambient noise are presented in the end.

Chapter 6 describes the different test structures used in the measurements.

Chapter 7 discusses the experimental results in detail. Different parameters such as bird's beaking, series connection in devices, operating region and bias dependence of flicker noise are discussed here with experimental results. A new algorithm for accurate extraction of flicker noise co-efficient (K_f) is shown successfully.

Chapter 8 includes the conclusions and future work.

CHAPTER 2

NOISE MODELING FUNDAMENTALS

2.1 Noise

When a system is built to measure or amplify small signals, one usually arrives at a lower signal limit of the system set by spontaneous fluctuations in current, voltage and temperature of the electronic components internal to the system under test. These spontaneous fluctuations are referred to as noise [1].

If the fluctuating voltage or current generated in an electronic device or circuit component is amplified by an ideal low-frequency amplifier and the amplified signal is fed into a loudspeaker, the loudspeaker produces a hissing sound. This hissing sound is perceived as noise and hence it is common practice to call the fluctuating currents and voltages "noise" even when no audible sound is produced. Because of its random nature, noise sets a fundamental lower bound on the detection capability of the system for which the signal can be successfully extracted from noise. Noise is an important topic in science and engineering since it sets a lower limit to the accuracy of any measurement that can be processed electronically.

2.1.1 Types of noise in electronic circuits and devices

Interference noise: Interference noise in an electronic circuit is the unwanted interaction between the circuit and the outside world or between different parts of the circuit itself. This type of noise may or may not appear as random signals. For example, power supply noise on ground wires(60 Hz hum) or electromagnetic interference between wires are deterministic noise whereas optical coupling of background light incident on a photo sensor is generally

random in nature. Interference noise can be significantly reduced by careful circuit wiring or layout, by shielding, or by changing the architecture of a system (for example, by using a battery so that 60Hz spikes are removed).

Inherent noise: Inherent noise is due to fundamental physical properties of electronic devices and specifically, due to the random nature of the movement of electrons in electronic components when current is flowing or not. It is random in nature and its effect can be minimized through judicious use of electronic devices and through the use of less noise sensitive circuit structures but it can never be eliminated.

2.1.2 Noise measures

Output and input referred noise: Noise is typically measured at the output of a circuit where the signal is usually the largest and easiest to measure. The significance of the noise performance of a circuit is, however, the limitation it places on the smallest input signals the circuit can handle before the noise unacceptably degrades the quality of the output signal. For this reason, the noise performance of a circuit is often expressed in terms of an equivalent input noise signal that appears at the input to a noiseless circuit which gives precisely the same output noise as the original circuit under consideration. The output noise is referred to the input by dividing the output noise signal by the power or voltage gain squared of the circuit. Both the input referred noise and the output noise can be either noise current or noise voltage. When referring an output noise back to the input, the amplifier gain can be a current gain, a voltage gain, a transresistance gain, or a transconductance gain depending upon the type of input source desired and the type of output noise signal characterized.

SNR: The power signal to noise ratio (SNR) of a node in a system is defined as

$$SNR \equiv 10\log\left[\frac{signal\ power}{noise\ power}\right] = 10\log\left[\frac{V_{x(rms)}^2}{V_{n(rms)}^2}\right] = 20\log\left[\frac{V_{x(rms)}}{V_{n(rms)}}\right] \quad (1)$$

where V_x is the signal voltage on the node and V_n is the noise voltage on the node. In the time domain, the total node voltage is given by the expression $V = V_x + V_n$.

Noise spectral density: The spectral density of a noise voltage source is defined as the mean square value of the source noise per unit bandwidth. It is equivalent to the average power per unit bandwidth that an identical voltage source would deliver to a load resistance of 1 Ω.

$$S_v = \frac{\overline{v_n^2}}{\Delta f} \quad (2)$$

where v_n is the rms value of the noise voltage whose time domain value is V_n.

Correspondingly, the spectral density of a noise current source is defined as the mean square value of source current noise per unit bandwidth. It is equivalent to the average power per unit bandwidth that an identical current source would deliver to a load resistance of 1 Ω.

$$S_i = \frac{\overline{i_n^2}}{\Delta f} \quad (3)$$

The total RMS voltage or current noise due to an element with noise spectral density S is given by the expression,

$$X_1 = \int_0^\infty S(f)df \quad (4)$$

where X_1 is an RMS current if $S=S_i$ or an RMS voltage if $S=S_v$. In a limited frequency band defined by $f_1 \le f \le f_2$, the total RMS noise voltage or noise current is given by the expression,

$$X_2 = \int_{f_1}^{f_2} S(f)df \quad (5)$$

In general, the spectral density is a function of frequency.

2.1.3 Noise sources in electronic devices

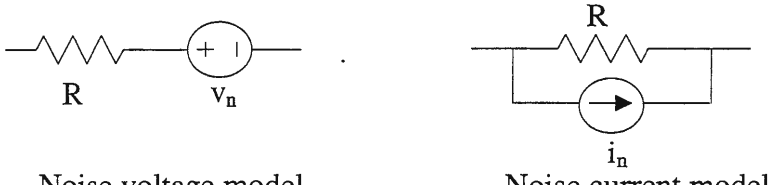
There are several mechanisms that contribute to noise in electronic devices. Both the type and magnitude of these mechanisms are dependent upon the type of electronic device and upon the operating conditions of the device. Five of the most common types of noise identified in electronic devices are Thermal noise, Shot noise, Flicker noise, Burst noise and Avalanche noise. A brief discussion of these basic noises follows [1,2,3,4].

Thermal noise: Thermal noise is due to the random thermal motion of the electrons in any resistive material and is unaffected by the presence or absence of direct current. It is also called white noise because its spectral density is constant i.e. not dependent on frequency. Since thermal noise source is due to the thermal motion of electrons, it is directly proportional to absolute temperature T and as T approaches zero, the thermal noise also approaches zero.

In a resistor, the thermal noise voltage spectral density is given by equation,

$$S_{v_{th}} = 4kTR \tag{6}$$

where R is the value of resistor, T is the temperature in Kelvin and k is Boltzmann's constant. A circuit model for the thermal noise source of a resistor is shown in Figure 2.1.



Noise voltage model Noise current model

Figure 2.1 - Thermal noise model

Equivalently, the thermal noise in the resistor can be modeled with a noise current source with spectral density

$$S_{i_{th}} = \frac{4kT}{R} \tag{7}$$

An equivalent circuit for the resistor with the noise current source is also shown in Figure 2.1.

Shot noise: Shot noise is generated by the random emission of electrons or by random passage of electrons and holes across a potential barrier. Shot noise is always associated with a direct-current flow and is present in diodes and bipolar transistors. The shot noise generated in a device is modeled by a parallel noise current source. The spectral density of the shot noise current is given by the expression

$$S_{i_{sh}} = 2qI \tag{8}$$

where q is the electric charge and I is the dc current flowing through the device. The spectral density of shot noise is also flat thus shot noise is white noise.

Flicker(1/f) noise: Flicker noise is a type of noise in which the spectral power density varies as a function of frequency. This frequency dependence is functionally of the form $1/f^{\gamma}$ where γ is close to one. Flicker noise is associated with a flow of direct current in electronic devices. There is not total agreement in the noise model community about the correct operating point dependence of flicker noise [5,6,7,8,9,10,11,12,13,14,15,16,17,18]. A commonly used model for circuit simulation (i.e. SPICE) for the spectral density of flicker noise is

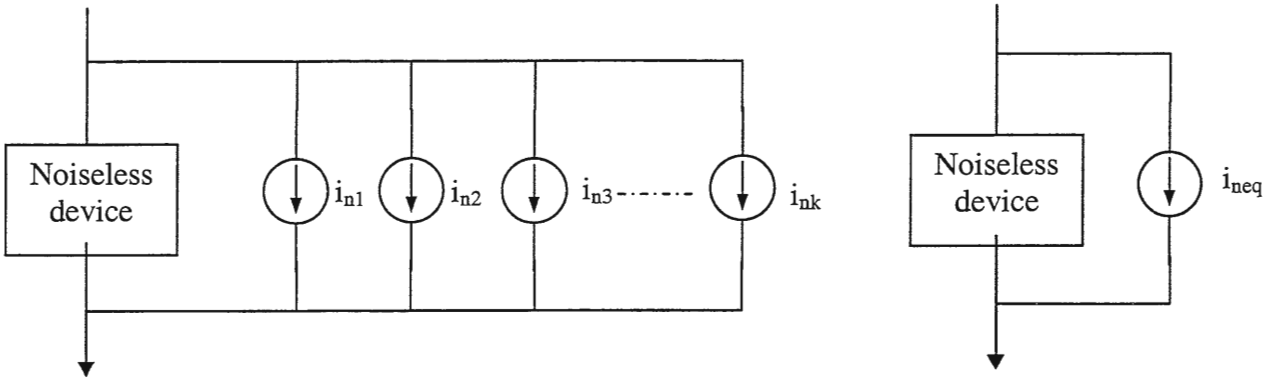
$$S_{i_f} = K_1 \frac{I^a}{f^{\gamma}} \tag{9}$$

where I is a direct current, K_1 is a constant that may depend upon device geometry for a particular device, a is a constant ranging from 0.5 to 2 and γ is a constant of about unity. This is the most basic model and is not discussed or used by noise physics researchers.

It is apparent that flicker noise is most significant at low frequencies although in devices exhibiting high flicker noise levels, this noise source may dominate the device noise at frequencies well into the megahertz range.

Electronic devices often exhibit several types of noise and the noise signals are generally uncorrelated. If each of the noise signals are characterized by noise currents between the same two nodes, then the overall noise is characterized by the circuit shown in Figure 2.2(a). The parallel noise current sources are equivalent to a single noise current source i_{neq} as depicted in Figure 2.2(b) where $i_{neq} = \sum_{j=1}^{k} i_{nj}$. If each current source has power spectral density S_{ij} and if all noise sources are uncorrelated, then i_{neq} is characterized by a spectral density

$$S_{ieq} = \sum_{j=1}^{k} S_{ij} \qquad (10)$$



(a) Multiple noise sources (b) Equivalent noise source

Figure 2.2 - Multiple Noise Sources in a device modeled as noise current sources between the same two nodes

A typical plot of the power spectral density for an element that contains both thermal and 1/f noise is shown in the Figure 2.3. The intersect of the asymptotic projection of the 1/f dominant source with the white noise dominant source is termed the 1/f noise corner.

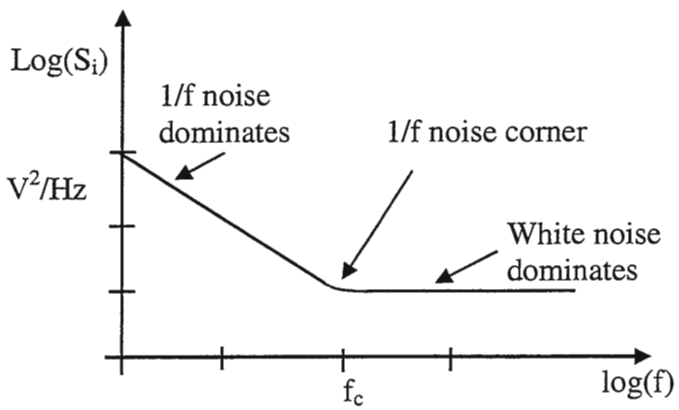


Figure 2.3 – Voltage noise spectral density for thermal and 1/f noise

Burst noise (Popcorn noise): Burst noise is a type of low frequency noise, which varies as $1/f^2$ at higher frequencies. The source of burst noise is not fully understood, but the source is related to the presence of heavy-metal ion contamination such as gold. Burst noise is so named for the fact that an oscilloscope trace of this type of noise shows burst of noise on a number (two or more) of discrete levels. The repetition rate of the noise pulses is usually in the audio frequency range and produces a "popping" sound when played through a loudspeaker and hence it is also called popcorn noise. The spectral density is of the form of,

$$S_i = K_2 \frac{I^c}{1+\left(\frac{f}{f_c}\right)^2} \tag{11}$$

where K_2 is a constant for a particular device, I is a direct current, c is a constant in the range 0.5 to 2 and f_c is a particular frequency for a given noise process. Note that this model is used for SPICE only.

Avalanche noise: Avalanche noise is produced by zener or avalanche breakdown in a pn junction. The holes and electrons in the depletion region must acquire enough energy to create hole-electron pairs by colliding with the lattice. This process is multiplicative and results in the production of a random series of noise spikes.

Typically 1/f noise and thermal noise are the major source of noise in MOS devices. Flicker noise (1/f) is dominant up through audio frequency range and thereafter, thermal noise becomes the dominant noise source. Shot noise, which is generated by gate leakage current and drain current in subthreshold MOS, is usually very small. It becomes significant only when the driving source impedance connected to the MOS gate is very large [2].

2.2 Consistency in models

2.2.1 Consistency

It is well known that two resistors of values R_1 and R_2 connected in parallel are equivalent to a single resistor of value $\frac{R_1 R_2}{R_1 + R_2}$ and the same two resistors when connected in series are equivalent to a single resistor of value R_1+R_2. Correspondingly, if second order effects are neglected, two MOS transistors M_1 and M_2 with width/length ratios of W_1/L_1 and W_2/L_2 when connected in parallel are equivalent to a single transistor with width/length ratio

$$\left(\frac{W}{L}\right)_{eq} = \frac{W_1 L_2 + L_1 W_2}{L_1 L_2} \tag{12}$$

and when connected in series with either M1 "above" M2 or M2 "above" M1, they are equivalent to a single transistor with width/length ratio

$$\left(\frac{W}{L}\right)_{eq} = \frac{W_1 W_2}{W_1 L_2 + L_1 W_2} \tag{13}$$

Similar equalities exist for the parallel or series connection of other devices such as diodes and BJT transistors.

Since there is still some disagreement about the modeling of even the most basic noise mechanisms in electronic devices, the issue of whether noise models applied to alternate and equivalent representations of a given device will predict the same noise performance in a circuit in which the device is used deserves consideration. We will hence introduce the following definition of consistency in noise models.

Definition: ***A noise model of a device is consistent if, when the noise model is applied to alternate and equivalent representations of the device, identical noise performance is obtained in any circuit in which the device is used.***

Since there are numerous possible alternate and equivalent representations of the device, we will generalize our definition for a consistent model and give an alternate definition for one of the equivalent representations of the device i.e. series-parallel combination of devices.

Alternate definition: ***For a particular noise model, if the noise performance for the series or parallel connection of two (or more) transistors is identical to that of a single equivalent transistor, it is called a consistent model.***

A noise model that is not consistent is termed an inconsistent noise model. At the outset, it may appear inconceivable that any noise model for a device would be proposed, much less utilized, that was inconsistent for at least two obvious reasons

1) An inconsistent model is inherently incorrect.
2) Attempts to use such a model would give different results for alternate equivalent representations of a circuit making it difficult to determine how to represent devices.

It is well known that the thermal noise model for a resistor is consistent. Conditions for consistency in thermal and 1/f noise models for MOS transistors will be developed. Finally, it will be shown later on in chapter 4 that popular and widely used thermal noise models and 1/f noise models for MOS transistors are inconsistent.

2.2.2 Consistency in thermal noise models for resistors

Equation (6) in section 2.1.3 shows the thermal model for resistors. With this noise model, it is shown in [2] that the thermal noise contributed by two resistors in series is equal to that of a single equivalent resistor. The same reference states that the noise of a parallel combination of two resistors is equal to that of the equivalent resistor. This supports the definition of consistency for this noise model.

2.2.3 Consistency in series connected devices

Inconsistency should not be confused with discontinuity in the transition between the saturation and triode regions. The issue of consistency can be best described by considering Figure 2.4.

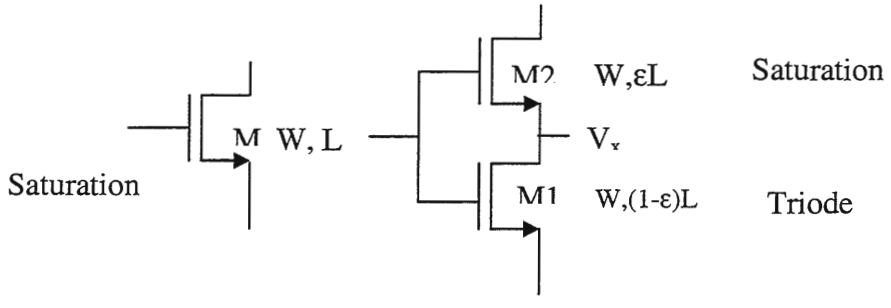


Figure 2.4 – Consistency problem in series connected devices

The device on the left is a single MOS transistor. The device on the right is two series connected transistors with a common gate. If lateral diffusion and short channel effects are neglected, both are identical for all ε, $\varepsilon \in (0,1)$.

Saturation Region Operation: If the square law model of Sah is used for device, it can be readily shown that if the single transistor has port voltages established to bias it in the saturation region, then the same port voltages will always place M1 in the triode region and M2 in the saturation region for all $\varepsilon \in (0,1)$. With a consistent model, the saturation region noise model for the single device of Fig. 2.4(a) can be obtained from a noise analysis of the structure of Fig. 2.4(b) with any $\varepsilon \in (0,1)$ where the triode region noise model is used for M1 and the saturation region model is used for M2. In particular, if ε is very nearly equal to 0, then essentially all of the noise is contributed by M1 and M1 is operating in the triode region. Thus, the noise in a consistent noise model will essentially be determined by the noise in a triode region device. It is interesting to note that most existing SPICE noise models of MOS transistors are developed directly in the saturation region, not in the triode region.

AC equivalence: Before deriving the noise relations between these transistors, we will first establish the ac equivalence between the two configurations of Figure 2.4(a) and 2.4(b). Assume that the aspect ratios of transistors M, M1 and M2 are W/L, W_1/L_1 and W_2/L_2.

From Figure 2.3, for equivalence between the two representations of M,

$$W1 = W2 = W \tag{14}$$

$$L1 = (1 - \varepsilon)\, L \tag{15}$$

$$L2 = \varepsilon\, L \tag{16}$$

Using the basic square law model for the transistors, from Sah's equations it follows that the drain current of M, M_1 and M_2 are given respectively by

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \qquad \text{Saturation} \tag{17}$$

$$I_{D1} = \beta_1 (V_{GS1} - V_T - \frac{V_{DS1}}{2}) V_{DS1} \qquad \text{Triode} \qquad (18)$$

$$I_{D2} = \frac{\beta_2}{2} (V_{GS2} - V_T)^2 \qquad \text{Saturation} \qquad (19)$$

Since M1 is in the triode region:

$$g_{m1} = \left. \frac{\partial I_{D1}}{\partial V_{GS1}} \right|_Q = \beta_1 V_{DS1}|_Q = \beta_1 V_{XQ}, \qquad (20)$$

$$g_{o1} = \left. \frac{\partial I_{D1}}{\partial V_{DS1}} \right|_Q = \beta_1 (V_{EB} - V_{XQ}) \qquad (21)$$

where V_{XQ} is the quiescent value of V_{DS1} and V_{EB} is the quiescent excess bias of M1.

Since M2 is in saturation:

$$g_{m2} = \beta_2 V_{EB2} \qquad (22)$$

Comparing the series connected port voltages to those of the equivalent single transistor, it follows that

$$V_{GS} = V_{GS1}$$

$$V_{GS} = V_{GS2} + V_X \qquad (23)$$

thus $$V_{GS} - V_T = V_{GS2} - V_T + V_X \qquad (24)$$

hence $$V_{EB} = V_{EB2} + V_X \qquad (25)$$

From [19],

$$V_{XQ} = V_{EB} \left(1 - \sqrt{\frac{L_2}{L_1 + L_2}} \right) \qquad (26)$$

and hence from (20), (21) and (22),

$$g_{m1} = \beta_1 V_{EB}\left(1-\sqrt{\frac{L_2}{L_1+L_2}}\right) \tag{27}$$

$$g_{o1} = \beta_1 V_{EB}\sqrt{\frac{L_2}{L_2+L_1}} \tag{28}$$

$$g_{m2} = \frac{\beta_2}{\beta_1} g_{o1} = \beta_2 V_{EB}\sqrt{\frac{L_2}{L_1+L_2}} \tag{29}$$

For the overall transistor M,

$$g_m = \beta V_{EB} \tag{30}$$

and hence from (27), (28), (29) and (30)

$$g_{m1} = \frac{\beta_1}{\beta}\left(1-\sqrt{\frac{L_2}{L_1+L_2}}\right) g_m \tag{31}$$

$$g_{o1} = \frac{\beta_1}{\beta}\sqrt{\frac{L_2}{L_1+L_2}}\, g_m \tag{32}$$

$$g_{m2} = \frac{\beta_2}{\beta}\sqrt{\frac{L_2}{L_1+L_2}} g_m \tag{33}$$

Observe that,

$$\beta = \mu C_{OX}\frac{W}{L} \tag{34}$$

$$\beta_1 = \mu C_{OX}\frac{W_1}{L_1} \tag{35}$$

and $$\beta_2 = \mu C_{OX}\frac{W_2}{L_2} \tag{36}$$

If we now assume W=W1=W2, it follows from (28), (35) and (36) that

$$\frac{\beta_1}{\beta} = \frac{W_1 / L_1}{W_1 / (L_1 + L_2)} = 1 + \frac{L_2}{L_1} \tag{37}$$

$$\frac{\beta_2}{\beta} = 1 + \frac{L_1}{L_2} \tag{38}$$

Defining $h = L_2/L_1$ (39)

it follows from (31), (32) and (33) that

$$g_{m1} = (1+h)\left(1 - \sqrt{\frac{h}{1+h}}\right) g_m \tag{40}$$

$$g_{o1} = \sqrt{(1+h)^2}\sqrt{\frac{h}{1+h}}\, g_m = \sqrt{h(1+h)}\, g_m \tag{41}$$

$$g_{m2} = \sqrt{\left(\frac{1+h}{h}\right)^2}\sqrt{\frac{h}{1+h}}\, g_m = \sqrt{\frac{1+h}{h}}\, g_m \tag{42}$$

From (40) and (41),

$$g_{m1} + g_{o1} = (1+h) g_m \tag{43}$$

Now, drawing a small signal equivalent circuit of the two series connected transistors with M1 in the triode region and M2 in the saturation region as

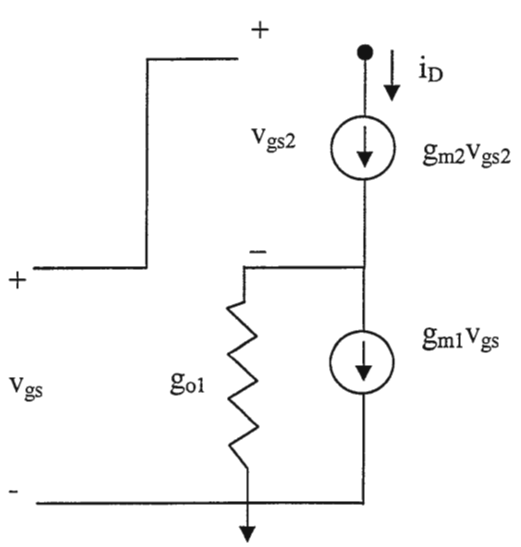


Figure 2.5 – Small signal equivalent circuit of series connected transistors

Lets check, if this is equivalent to a small signal model of a single transistor. From Figure 2.5

$$i_D = g_{m2} v_{gs2} \tag{44}$$

$$v_{gs} = v_{gs2} + \frac{\left(g_{m2} v_{gs2} - g_{m1} v_{gs}\right)}{g_{o1}} \tag{45}$$

and hence,

$$v_{gs}(g_{o1} + g_{m1}) = v_{gs2}(g_{o1} + g_{m2}) \tag{46}$$

substituting v_{gs2} from (46) into (45),

$$i_D = g_{m2} v_{gs} \left(\frac{g_{o1} + g_{m1}}{g_{o1} + g_{m2}} \right) = \hat{g}_m v_{gs} \tag{47}$$

where $\hat{g}_m = g_{m2} \left(\frac{g_{o1} + g_{m1}}{g_{o1} + g_{m2}} \right)$ (48)

substituting the values from (40), (41), (42) and (43)

$$\hat{g}_m = g_m \left[\frac{(1+h) g_m}{\sqrt{h(1+h)} + \sqrt{\frac{1+h}{h}}} \right] \left[\sqrt{\frac{1+h}{h}} \frac{1}{g_m} \right]$$

simplifying the equation above we get $\hat{g}_m = g_m$

Noise equivalence: Assuming saturation region operation and neglecting the small signal output conductance, the small signal equivalent circuit for the single transistor M of Figure 2.4 is shown in Figure 2.6 is obtained.

The noise equivalent circuit for M1 and M2 of Figure 2.4 is shown in the Figure 2.7, where i_{n1} and i_{n2} are the noise currents of the M1 and M2 respectively. As stated previously, M1 is operating in the triode region and M2 is operating in the saturation region. The output

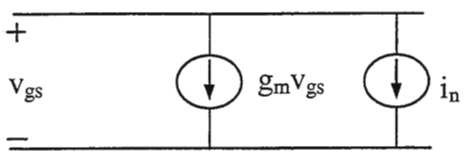


Figure 2.6 - Noise equivalent circuit of a single MOS transistor

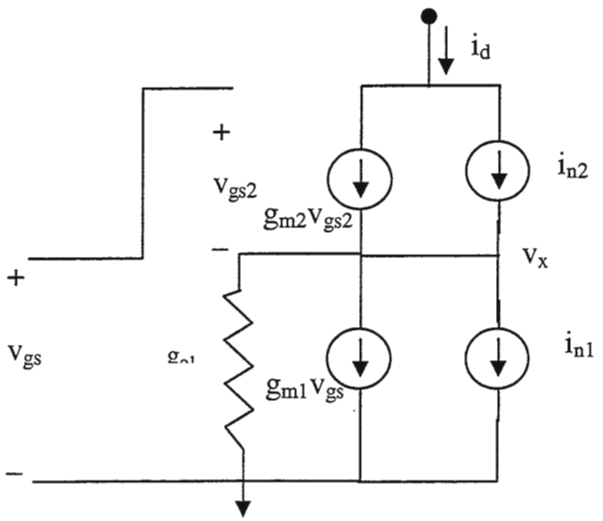


Figure 2.7 - Noise equivalent circuit for series connected transistors

conductance of M2 has been neglected in this model. Since the series combination of M1 and M2 is equivalent to the single transistor M, relationships exists between the parameters in Figure 2.6 and those in Figure 2.7. These relationships will now be derived. For the circuit of Figure 2.7 small signal equations can be written as,

$$i_d = g_{m2} v_{gs2} + i_{n2} \tag{49}$$

$$i_{n2} + g_{m2} v_{gs2} = g_{m1} v_{gs} + g_{o1} v_x + i_{n1} \tag{50}$$

$$v_{gs} = v_{gs2} + v_x \tag{51}$$

and hence,

$$i_{n2} + g_{m2} v_{gs2} = g_{m1} v_{gs} + g_{o1}(v_{gs} - v_{gs2}) + i_{n1} \tag{52}$$

and $$v_{gs2} = \frac{i_{n1} - i_{n2} + v_{gs}(g_{m1} + g_{o1})}{g_{m2} + g_{o1}} \tag{53}$$

Substituting this value of v_{gs2} into (49),

$$i_d = i_{n2} + \frac{g_{m2}}{g_{m2} + g_{o1}}(i_{n1} - i_{n2}) + g_{m2}\left(\frac{g_{m1} + g_{o1}}{g_{m2} + g_{o1}}\right) v_{gs} \tag{54}$$

$$= i_{n1}\left(\frac{g_{m2}}{g_{m2} + g_{o1}}\right) + i_{n2}\left(\frac{g_{o1}}{g_{m2} + g_{o1}}\right) + g_{m2}\left(\frac{g_{m1} + g_{o1}}{g_{m2} + g_{o1}}\right) v_{gs} \tag{55}$$

and from (48) this equals,

$$i_d = i_{neq} + \hat{g}_m v_{gs} \tag{56}$$

where rms value of of i_{neq} is given by the expression,

$$i^2_{neq,rms} = \left(\frac{g_{m2}}{g_{m2} + g_{o1}}\right)^2 i^2_{n1,rms} + \left(\frac{g_{o1}}{g_{m2} + g_{o1}}\right)^2 i^2_{n2,rms} \tag{57}$$

and where the spectral density of i_{neq} is given by,

$$S_n = \left(\frac{g_{m2}}{g_{m2} + g_{o1}}\right)^2 S_{Tn1} + \left(\frac{g_{o1}}{g_{m2} + g_{o1}}\right)^2 S_{n2} \tag{58}$$

where S_n, S_{Tn1} and S_{n2} are the current power spectral densities of n, n1 and n2 respectively. We have used the subscript " T " to emphasize the fact that S_{Tn1} refers to the triode region spectral density. Throughout the remainder of the thesis, a subscript of " T " on a spectral density will denote a triode region spectral density. A spectral density without a subscript "T" will indicate saturation region operation.

From (27), (28), (29), (39) and (58) these consistency relationships can be expressed equivalently as

$$S_n = \frac{1}{(1+h)^2} S_{Tn1} + \left(\frac{h}{1+h}\right)^2 S_{n2} \tag{59}$$

But from Figure 2.4 and (39) it follows that,

$$h = \frac{\varepsilon}{(1-\varepsilon)} \tag{60}$$

Thus, from (59) and (60) S_n can be rewritten as

$$S_n = (1-\varepsilon)^2 S_{Tn1} + \varepsilon^2 S_{n2} \tag{61}$$

Correspondingly, it follows directly from (55) that g_m of Figure 2.6 relates to the parameters in the circuit of Figure 2.7 by the relation

$$g_m = g_{m2}\left(\frac{g_{m1} + g_{o1}}{g_{m2} + g_{o1}}\right) \tag{62}$$

Triode Region Operation: If M1 and M2 in Figure 2.4 are both operating in the triode region, the noise equivalent circuit of the single transistor and the two-transistor implementations are as shown in Figure 2.8 (a) and (b) respectively. Note that g_m and g_o values are now for the triode region operation as given by (20) and (21).

A straightforward but tedious analysis will give the relationship between the parameters in Figure 2.8 (a) and those of the equivalent circuit of Figure 2.8 (b). These results are summarized below.

$$i_d = \left(\frac{g_{m1}g_{m2} + g_{m1}g_{o2} + g_{m2}g_{o1}}{g_{o1} + g_{o2} + g_{m2}}\right) v_{gs} + \left(\frac{g_{o1}g_{o2}}{g_{o1} + g_{o2} + g_{m2}}\right) v_{ds}$$

$$+ \left(\frac{g_{o2} + g_{m2}}{g_{o1} + g_{o2} + g_{m2}}\right) i_{n1} + \left(\frac{g_{o1}}{g_{o1} + g_{o2} + g_{m2}}\right) i_{n2} \tag{63}$$

From this, it follows from a simple analysis of the circuit of Figure 2.8 (b) that

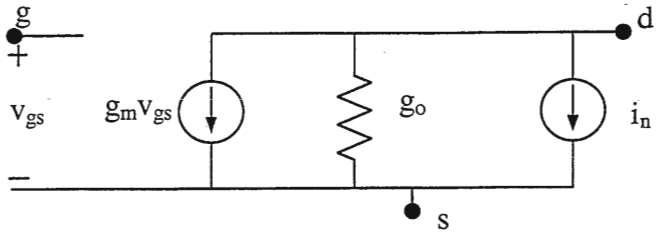


Figure 2.8 (a) - Triode region small signal noise model of MOSFET

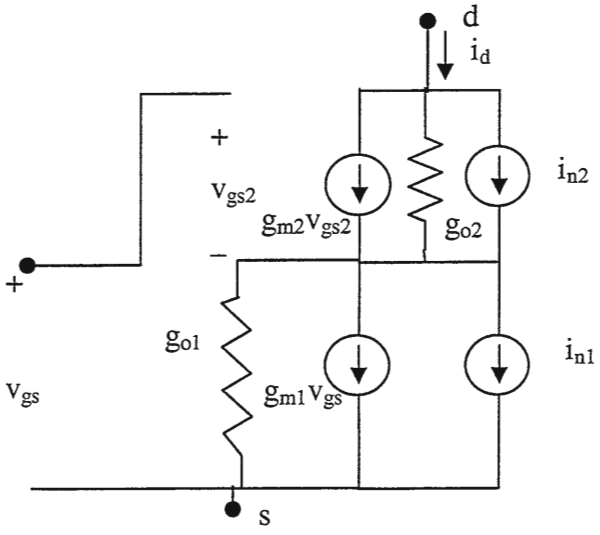


Figure 2.8 (b) - Two transistor noise model of MOSFET in triode region

$$g_m = \frac{g_{m1}g_{m2} + g_{m1}g_{o2} + g_{m2}g_{o1}}{g_{o1} + g_{o2} + g_{m2}} \tag{64}$$

$$g_o = \frac{g_{o1}g_{o2}}{g_{o1} + g_{o2} + g_{m2}} \tag{65}$$

$$S_{Tn} = \left(\frac{g_{o2} + g_{m2}}{g_{o1} + g_{o2} + g_{m2}}\right)^2 S_{Tn1} + \left(\frac{g_{o1}}{g_{o1} + g_{o2} + g_{m2}}\right)^2 S_{Tn2} \tag{66}$$

where S_{Tn}, S_{Tn1} and S_{Tn2} are the spectral densities of M, M1 and M2 respectively.

Substituting the dc operating point dependence in (66) as obtained from the Sah model, it follows that

$$S_n = (1-\varepsilon)^2 S_{Tn1} + \varepsilon^2 S_{Tn2} \tag{67}$$

Observe by comparing (61) and (67) that this is identical to the functional form of the relationship that was developed for saturation region operation.

Several observations about consistency in device models can be made. The first if the relationship between the triode region and the saturation region noise models and the effects of V_{ds} on the noise when a device is operating in the saturation region. From (61), for very small ε, it follows that

$$S_n = S_{Tn1}\big|_{Vds1=VEB} \tag{68}$$

When a transistor is operating in the saturation, it follows from (20), (21) and (26) that the drain-source voltage of M1 is given by,

$$V_{ds1} = V_{EB}\left(1-\sqrt{\varepsilon}\right) \tag{69}$$

Thus for ε very small, V_{ds1} is independent of the drain-source voltage of M. It thus follows from (68) that S_n is not dependent upon the saturated drain-source voltage and is totally dependent upon the triode-region noise characteristics. It is thus sufficient to model the noise of a MOS transistor in the triode region and then use (68) to obtain the saturation region noise model.

A second observation relates to the functional form of the device model.

Thus, if a noise model is consistent, the relationship of (58) must be satisfied for all ε in (61) or correspondingly for all h in (59).

2.2.3 Consistency in parallel connected devices

Similar to series connected case, total noise in parallel combination of transistors should be equal to that of a single equivalent transistor if effective W/L and effective device current is held constant. Hence for consistent noise model, total noise in Figure 2.9 should be

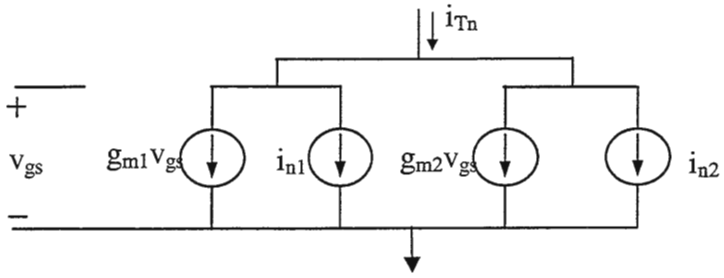


Figure 2.9 – Consistency in parallel connected devices

$$i_n = i_{n1} + i_{n2} \tag{70}$$

and hence,

$$i_{T_n,rms} = \sqrt{i_{n1,rms}^2 + i_{n2,rms}^2} \tag{71}$$

and the current power spectral densities satisfy the relationship

$$S_n = S_{n1} + S_{n2} \tag{72}$$

Thus, equations (59), (61) and (71) give the equivalent noise spectral density relationships for series and parallel connected devices for a consistent noise model. The results for the two transistors case can be easily extended to n transistors. Generalized noise relations for n parallel connected (bipolar and MOS) transistors can be found in [20].

We will be proving our hypothesis of consistency definition for thermal and flicker noise in chapter 4. It will be shown there in detail that widely used models for thermal and flicker noise are grossly inconsistent.

CHAPTER 3

BACKGROUND ON 1/F NOISE

3.1 1/F noise observations

Engineering interest in the low-frequency (1/f) noise behavior of submicron Si MOSFETs is driven by analog applications, where noise minimization is a key issue and often defines the sensitivity or detection limit of the system. Low frequency noise is strongly technology dependent and in some cases it can be used as a predictive or diagnostic tool for device lifetime and reliability [11,12,21].

Flicker (1/f) noise is an excess noise found to some extent in all types of transistors and some types of resistors. Flicker noise has various origins; In bipolar transistors it is caused mainly by traps associated with contamination and crystal defects at the base emitter junction [22]. In MOSFETs, it is caused by tunneling mechanism as well as mobility fluctuations. Whatever the cause, flicker noise is definitely not white or even truly Gaussian. To a first approximation, flicker noise contains equal amounts of energy in each decade of bandwidth. This gives it a power spectrum inversely proportional to frequency and hence it is called 1/f noise. As frequency decreases, flicker noise starts to dominate the noise spectrum and the frequency at which flicker noise starts to become dominant is generally known as the 1/f 'noise corner'. Noise current contributes to the total drain current and is modeled as a current source between drain and source. In this thesis, we will focus on 1/f noise in MOS transistors. The equivalent contribution, as a noise power voltage spectral density source at the input of a MOS transistor in series with gate can be obtained by dividing the drain power

voltage noise current by the g_m^2 of the transistor. The two alternate and equivalent small signal models for the 1/f noise of a MOSFET is shown in figure 3.1.

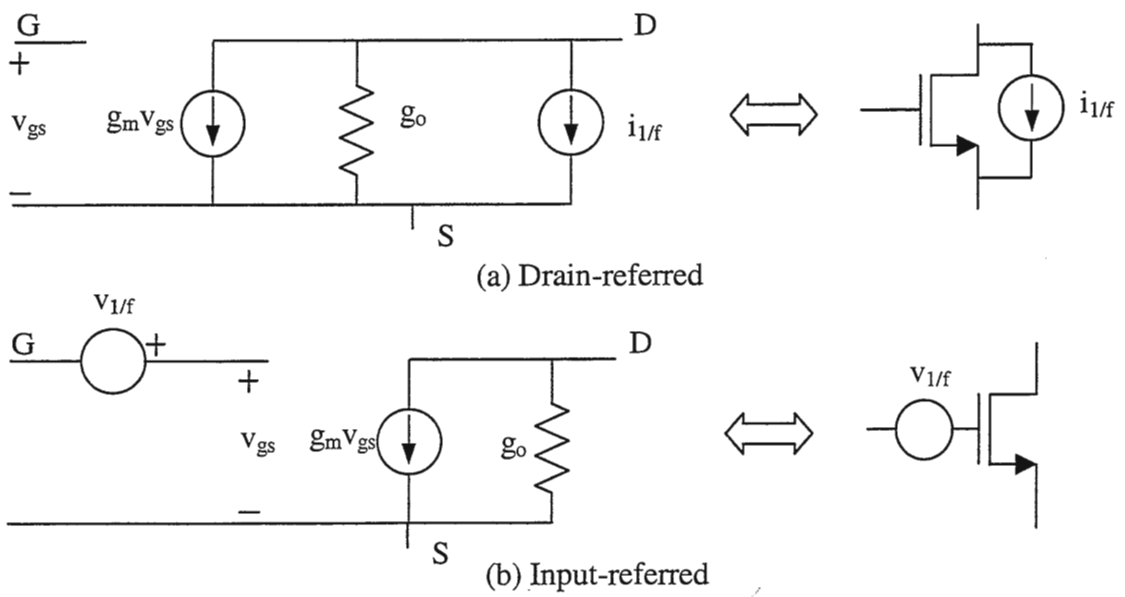


Figure 3.1 - Models of 1/f noise in a MOS transistor

There is still a considerable gap between the recent advances in the physical understanding of the origin of 1/f noise in CMOS transistors and the requirements of the design engineer who needs to optimize the 1/f noise of the transistors.

3.2 Physical mechanisms governing 1/f noise

There are several theories for the origin of 1/f noise, with involved physics and sometimes conflicting conclusions. Several issues about 1/f noise remain unresolved. The flicker noise in MOSFETs has been studied since the mid 1950s. Since 1990-92, there is strong agreement among the researchers on the physical mechanisms responsible for this noise. Almost all researchers accept it as a number fluctuation theory, however models are still a problem. There are no widely accepted quantitative models for it for analytical purposes and in the circuit simulators.

The 1/f noise is termed as fluctuation in conductivity.

Conductivity $\sigma = nq\mu$

Where n = electron concentration (electron per cubic meter), μ = mobility and q = charge. So, question is what is fluctuation with a 1/f spectrum: n (number) or μ(mobility)? At present, there are two major theories to explain the physical origins of 1/f noise in MOSFETs. One is the number fluctuation model based on the McWhorter's [6] charge trapping model; the other is the bulk mobility fluctuation theory based on Hooge's hypothesis [7,23]. The Hooge model is not accepted as a physical model but is used as a circuit model. Extensive noise data have been reported and interpreted with both models.

3.2.1 Number fluctuation model (Carrier density fluctuation model) [6,9,24]

Defects at or near the critical Si/SiO_2 interface can increase the 1/f noise and reduce the yield, performance, and reliability of MOSFET devices. Different kinds of defects at and near the Si/SiO_2 interface of MOS devices can be found in detail in [24].

Traps located at ~15 A° into oxide (1 Hz traps) can often exchange charge via tunneling or thermally activated processes with the underlying Si on time scales of order of 1 s or less.

A commonly used model for the spectral density of flicker noise is

$$S_{i_f} = K_1 \frac{I^a}{f^\gamma} \qquad (1)$$

where I is a direct current, K_1 is a constant that may depend upon device geometry for a particular device, a is a constant ranging from 0.5 to 2 and γ is a constant of about unity.

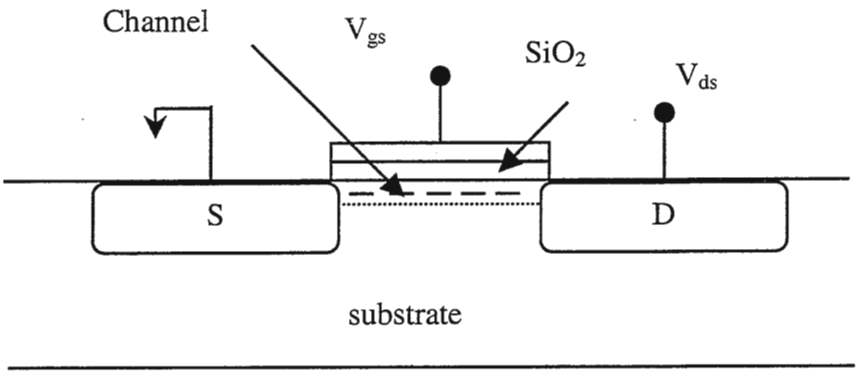


Figure 3.3 - Cross section of MOS transistor explaining number fluctuation

The flicker noise is attributed to the random trapping and detrapping processes of charges in the oxide traps near the Si-SiO_2 interface via tunneling. The channel region susceptible to tunneling is shown in the cross section of MOS transistor in the Figure 3.3. The charge fluctuation results in fluctuation of the surface potential, which in turn modulates the channel carrier density. Mathematically it can be shown that [13] a uniform energy distribution of oxide traps near the interface will give rise to a distribution of time constants which add up to yield the 1/f noise spectrum.

This model treats noise as a surface effect rather than bulk effect.

3.2.2 Mobility fluctuation model [7,23]

This theory attributes flicker noise to mobility fluctuations, due to carrier interactions with lattice fluctuations. An empirical relation for 1/f noise in homogeneous samples is

$$S_I = \frac{\alpha}{fN} I^2 \qquad (2)$$

where S_I is the current spectral density for a wide range of materials, f the frequency, N the total number of electrons (or holes) and α is a dimensionless constant termed as Hooge's constant. $\alpha=2x10^{-3}$ is a universal constant of the Hooge's model and this value has never

been measured in any semiconductor. The dependence of α on μ can be found from a set of carefully prepared samples, where only one parameter is varied. The dimensions length, width and thickness do not appear in (2), proving that 1/f noise is a bulk effect. This noise is a fluctuation in mobility. Several modifications to original equation (2) have been proposed thereafter.

3.2.3 Combination of both models and some other speculations

Some research indicated indicated in the past that flicker noise is due to both carrier number fluctuation and mobility fluctuation [8,11,13] however it is not considered fundamental today according to physicists. The carrier number fluctuation theory talks about a randomly varying charge at traps near the interface, and that charge can affect mobility through "Coulomb scattering" and hence both effects may be present and correlated in a given device. Many mathematical model based experiments in the past have suggested that 1/f noise in n-MOSFETs is dominated by number fluctuation while in p-MOSFETs it is dominated by mobility fluctuation [8,13]. However, the references [8,11,13] are not physics based references, but they are mathematical models. Mobility is not accepted as a physical model in MOS any longer.

Random telegraph noise: If a transistor gate area (width (W) times length (L) – WL) is very small, the flicker noise can be expected to be high. This is because there will now be only a few traps which can exchange charge with the channel, and their individual effect will be noticed, rather than tending to average out as in the case of large gate area. It is, in fact, possible that only a single trap of this type exists in a very small device. Then, as it captures and releases charge, abrupt changes in the drain current can be noticed as shown in Figure

Figure 3.4 - Variation of drain current due to Random Telegraph Noise

3.4. These changes will be on top of the more common noise variation. This is reminiscent of the so called "random telegraph signals" (RTS) in communication theory, and hence it is often called random telegraph noise [5,14,15,25]. Analysis of the amplitude of the current fluctuations reveal that the oxide traps generate noise by modulating the carrier number, as well as the carrier mobility through Coulomb scattering. Flicker noise observed in large dimension devices has been viewed as a superposition of many RTS waveforms [25].

P-channel noise: For n+ gate process, flicker noise power spectral densities in p-channel devices are generally found to be significantly less than those of n-channel devices of the same dimensions and fabricated with the same CMOS process (by 1 order of magnitude or more), unless $|V_{GS}-V_T|$ is very large, in which case the two types of devices may give similar noise [26]. For p+ gate process p-channel device can have flicker noise coefficient (K_f) about the same or from ½ to 2x the n-channel device. The low value of flicker noise in p-channel device for n+ gate process is attributed to the fact that the channel is farther away from the Si-SiO_2 interface and thus is less affected by interface traps. Different tunneling barrier

heights for electrons and holes, different oxide trap density near the conduction and valence bandedge, and different electron and hole mobility results in different degree of number fluctuation in n and p-channel devices. If process is too noisy, p-channel device could have higher noise than n-channel device but usually it is not the case.

3.3 Existing 1/f noise models

Several fundamentally different circuit models for the 1/f noise in MOS transistors have appeared in the literature. Although these have evolved over the years, there is invariably insufficient experimental data to validate any of these models. Some of the more commonly used models are summarized in this section.

In all cases, the 1/f noise is modeled as a noise current source from drain to source as depicted in the small signal model of Figure 3.1 (a). The noise current source in all cases is characterized by the current spectral density (A/√Hz). The subscripts $_{SAT}$ and $_{TRIODE}$ denote the saturation and triode regions respectively.

HSPICE Models: The user can use the parameter NLEV [16] to select one of three 1/f noise models. The two parameters KF and AF are termed the flicker noise coefficient and flicker noise exponent respectively. The parameter I_{ds} is quiescent drain current, C_{ox} is the gate oxide capacitance density, W_{eff} is the effective width and L_{eff} is the effective length. Default values of KF, AF and NLEV are 0,1 and 2 respectively. The current spectral densities are given in saturation and triode regions by the expressions

$$\text{NLEV=0, } S_{1/f\,TRIODE} = S_{1/f\,SAT} = \frac{KFI_{ds}{}^{AF}}{C_{OX} L_{eff}^2 f} \quad \frac{A^2}{Hz} \tag{3}$$

$$\text{NLEV=1, } S_{1/f\,TRIODE} = S_{1/f\,SAT} = \frac{KFI_{ds}{}^{AF}}{C_{OX} W_{eff} L_{eff} f} \quad \frac{A^2}{Hz} \tag{4}$$

$$\text{NLEV=2,3}\quad S_{1/f\,TRIODE} = S_{1/f\,SAT} = \frac{KF g_m{}^2}{C_{OX} W_{eff} L_{eff} f^{AF}} \quad \frac{A^2}{Hz} \tag{5}$$

Note that there are fundamental differences in even the functional form of the spectral densities. The parameter KF has units (if AF=1) of AF(ampere•farads) in (3) and (4) whereas it has units V^2F in (5). The flicker noise exponent AF is an exponent for the quiescent drain current in (3) and (4) and an exponent of f^{-1} in (5). If AF≠1, the units of KF in (3) and (5) differ even more.

Aside from the unfortunate use of identical parameters to denote different effects in (3) and (5), the expressions of (3) and (5) are approximately the same if AF≅ 1. This can be seen by observing that

$$g_m \cong \sqrt{\frac{\mu C_{OX} W_{eff}}{L_{eff}} 2\sqrt{I_{ds}}} \qquad \text{SATURATION} \tag{6}$$

$$g_m \cong \frac{\mu C_{OX}}{L_{eff}} V_{ds} \qquad \text{TRIODE} \tag{7}$$

where μ is the channel mobility.

Substituting this equation into (5) we obtain,

$$S_{1/f\,SAT}\ (AF=1) \cong \frac{[KF \cdot 2\mu] I_{ds}}{L_{eff}^2 f} \quad \frac{A^2}{Hz} \tag{8}$$

Thus the parameter KF in (3) and (5) relate by $KF_{(3)} = KF_{(5)} \cdot 2\mu$

An additional fundamental distinction associated with device geometry exists when comparing (3) and (4). In particular, (3) predicts the spectral density is dependent only upon L_{eff}^2 (i.e. independent of W_{eff}) and thus is independent of area whereas (4) implies a fundamental dependence on channel area.

Hiroaki Mikoshiba '82 [8]: This model is a combination of the number and mobility fluctuation models. For the linear (triode) region of operation equivalent gate noise voltage spectral density is given by,

$$S_{vnG}(f) = \frac{1}{LWf}\left[K_1\left(\frac{q}{C_{ox}}\right)^m (V_G - V_T) + K_2\left(\frac{q}{C_{ox}}\right)^2\right] \tag{9}$$

where $K_1 = \frac{\alpha_{inv}}{(1-\gamma)^2} = mobility\ term\ and\ K_2 = \frac{N_{to}(E_F)kT}{\beta(1-\gamma)^2} = number\ \text{term}$,

α_{inv} is Hooge's parameter in surface inversion layers, m=0.7-1.2, $N_{t0}(E_F)$ = oxide trap density at Fermi-level, $\beta = (4\pi/h)\sqrt{2m^* E_B}$, m^* is effective electron mass, h is Planck's constant and E_B is barrier height. Mobility term K_1 is shown proportional to $\sqrt{K_2}$ but correlation is not clearified.

Raj Jayaraman and Charles Sodini '89 [11]: This model is also a combination of number and mobility fluctuation model. For linear region of operation,

$$S_{V_G} = S_{V_{G1}} + S_{V_{G2}} + S_{V_{G3}} \tag{10}$$

where $S_{V_{G1}} = \frac{kTq^2}{8WLC_{ox}^2\alpha}\frac{N_t(E_{fn})}{f}$ (11)

$$S_{V_{G2}} = \frac{kTq^2}{WL}\int \frac{2S(x)\mu_N(V_{GS}-V_T)}{C_{OX}}\frac{\tau_T(x)}{1+w^2\tau_T^2(x)} \bullet N_t(E_{fn})dx \tag{12}$$

$$S_{V_{G2}} = \frac{kTq^2}{WL}\int S^2(x)\mu_N^2(V_{GS}-V_T)^2\frac{\tau_T(x)}{1+w^2\tau_T^2(x)} \bullet N_t(E_{fn})dx \tag{13}$$

where $N_t(E_{fn})$ is the oxide trap density adjacent to the electron quasi-Fermi level in silicon, $\alpha = \sqrt{\frac{2m_e^*\phi_B}{h^2}}$ where m* is the effective mass of the electron in the oxide, h is Planck's

constant divided by 2π, ϕ_B is the height of the oxide conduction band edge from the Si conduction band edge, μ_N is the time average mobility, S(x) is the scattering rate and τ_T is the time constant associated with a trapping event. The term S_{VG1} is pure number fluctuation term, S_{VG3} is a pure mobility term and S_{VG2} is a cross product term between number fluctuations and mobility fluctuations

Kwok K. Hung, Ping Ko, Chenming Hu and Yiu Cheng '90 [13]: This model is also a combination of number and mobility fluctuation model and for low drain voltages, drain current referred noise power is given by,

$$S_{I_d}(f) = \frac{kTI_d^2}{\gamma f WL}\left(\frac{1}{N} + \alpha\mu\right)^2 N_t(E_{fn}) \tag{14}$$

where N is the number of channel carriers per unit area, μ is the carrier mobility, q is the electron charge, N_t is the number of occupied traps per unit area, $N_t(E_{fn})$ is the oxide trap density adjacent to the electron quasi-Fermi level in silicon, I_d is the drain current, γ is the attenuation coefficient of the electron wave function in the oxide given by

$\gamma = (4\pi / h)\sqrt{2m^* \varphi_B}$ where m* is the effective mass of the carrier in oxide, h is Planck's constant and ϕ_B is the tunneling barrier height seen by the carriers at the interface. γ is typically taken to be 10^8 cm^{-1}.

Dividing (14) by the square of the transconductance ($g_m = \partial I_d / \partial V_g = W\mu C_{OX} V_d / L$), V_d being the drain voltage) yields the input referred noise power,

$$S_{I_d}(f) = \frac{kTq^2}{\gamma f WLC_{OX}^2}(1 + \alpha\mu N)^2 N_t(E_{fn}) \tag{15}$$

Flicker noise power at an arbitrary drain bias is given by,

$$S_{Id}(f) = \frac{kTq^2 I_d \mu_{eff}}{a\gamma f L^2 C_{OX}} \left[A \ln \frac{N_0}{N_L} + B(N_0 - N_L) + \frac{1}{2} C(N_0^2 - N_L^2) \right] \quad (16)$$

where $qN_0 = qN(0) = C_{OX}(V_g - V_{th0})$ (17)

and $qN_L = qN(L) = C_{OX}(V_g - aV_d)$ (18)

where N_0 and N_L are carrier densities at the source and drain ends of the channel, A, B and C are technology dependent model parameters.

Z. -H. Fang, A. Chovet, Q.-P. Zhu and J. –N. Zhao '91 [9]: This is a number fluctuation model. For all regions of operation, the drain current spectral density is given by the equation,

$$S_{ID} = Kd_t N_t(E_F) \frac{1}{16f} \quad (19)$$

where $K=K_0*I_0$, $N_t(E_F)$ is the trap density in the oxide, E_F is the Fermi level at the equilibrium. K_0 and I_0 are given by the relation,

$$K_0 = \frac{4I_D^2 \beta^2 q^2}{L^2 W} \delta^2 \quad (20)$$

$$I_0 = \int_0^L \frac{dx}{(C_{OX} + C_{it} + C_n + C_d)^2} \quad (21)$$

where, I_D is the drain current, β = q/kT (q is the electronic charge, k the Boltzmann's constant and T the absolute temperature), L the channel length, W the channel width. C_{ox}, C_{it}, C_n and C_d are respectively, the oxide, interface state, charge channel and depletion capacitance per unit area. δ=1 for strong inversion and δ=1/2 for weak inversion.

Y. Zhu, M. J. Deen and T. G. M. Kleinpenning '92 [17]: This model is a mobility fluctuation model. In saturation region of operation, gate referred 1/f noise voltage spectral density in V^2/Hz is

$$S_{VG}(f) = \frac{2\alpha q(V_{GS} - V_T)L'\left[1-(1-L''/L')^{1/2}\right]}{f\ddot{Z}^2 WC_{OX}} \quad where\ \ddot{Z} = L''-\mu_{eff} I_D / Zv_x \quad (22)$$

and $Z = -v_x W\left(C_{ox} + \frac{1}{2}\{2\in_{Si} qN_A/[V(L'') + 2\Phi_F]\}^{1/2}\right)$, L' is the channel position from source where the potential is V_{GS}-V_T, L" is the position from source junction at which the numbers of free electrons in the channel and the electrons in depletion region are equal, α is the effective Hooge's parameter and $\alpha = \left(\frac{\mu_{eff}}{\mu_{latt}}\right)^2 \alpha_H$, α_H is a dimensionless constant of about $2x10^{-3}$ (Hooge's constant), v_x is the saturation velocity in cm/s, C_{ox} is the gate oxide capacitance in unit area (F/cm^2), W is the channel width, ε_{Si} is the permittivity of silicon (F/cm), N_A is the substrate doping concentration (cm^{-3}) and φ_F is the Fermi level potential (V).

John Scofield, Nick Borland and Daniel Fleetwood '94 [18]: This model shows n-channel device as a number fluctuation and p-channel device as a mobility fluctuation . For linear region of operation with constant I_d and V_g,

$$S_{Vd}(f) \approx \frac{V_d 2}{(V_g - V_{th})2}\frac{e2}{C_{ox}^2}\frac{k_b TD_t}{LWf\ln(\tau_1/\tau_0)} \quad (23)$$

where V_{th} is the threshold voltage, Id is the drain current, Vg is the gate voltage, e is the fundamental unit of charge, k_b is Boltzmann constant, T is absolute temperature, LW is the gate area, C_{ox} is the gate oxide capacitance per unit area, D_t is the number of traps per unit

energy per unit gate area, $\tau 1$ and $\tau 2$ are minimum and maximum tunneling times associated with maximum and minimum tunneling distances assumed for the trap distribution.

L. K. J. Vandamme, Xiaosong Li and Dominique Riguad Nov '94 [12]: This model shows n-channel device as a number fluctuation and p-channel device as a mobility fluctuation. Below saturation ($V < V_s$) with V_s the drain saturation voltage,

$$S_I = \frac{\alpha q \mu^2 C_{ox} V_G^{*} V^2 W}{f L^3} \propto \frac{W}{L^3} \tag{24}$$

where α is a volume and device-length independent 1/f noise parameter between 10^{-7} and 10^{-3}, q is the elementary charge, μ is the mobility, V_G^* is the effective gate voltage, V is the drain voltage, C_{ox} is the oxide capacitance per unit area, W and L are the channel width and length respectively. For saturation region,

$$S_I = \frac{\alpha q \mu^2 C_{ox} V_G^{*3}}{2} \frac{W}{L^3} \propto \frac{W}{L^3} \text{ if constant } V_G^* \tag{25}$$

C. Jackobson, I. Bloom and Y. Nemirovsky '98 [10]: This is a number fluctuation model. In the linear region of operation,

$$S_{Id}(f) = \frac{q^2}{C_{ox}^2} \left(\frac{I_d}{V_g - V_t} \right)^2 \frac{N_{ot}}{WL} \frac{1}{f} \tag{26}$$

where q is the elementary charge, C_{ox} is the oxide capacitance per unit area, I_d is the drain current, N_{ot} is the equivalent density of oxide traps per unit area, V_g is the gate voltage, V_d is the drain voltage. For saturation region of operation,

$$S_{Id}(f) \cong \frac{q^2 \mu N_{ot} I_d}{C_{ox}^2 L_{eff}^2} \frac{1}{f} \tag{27}$$

where μ is the channel mobility and L_{eff} is the channel length.

A detailed review of most of the models published in literature so far can be found in [5].

3.3.1 Assessment of existing models

As we see from above equations, there exists a fundamental lack of understanding of even basic 1/f noise models among the design community. Extensive models have been published for theories based upon both the number fluctuation and mobility fluctuation approach. Researchers have combined the carrier-density fluctuation model and mobility fluctuation model in an uncorrelated [8] or correlated [11] manner, to explain the noise mechanism. The validity of these models for large feature size devices has not been established and the understanding for submicron devices is even less mature yet. Inconsistent experimental results were reported for both n- and p-channel devices. Most of the 1/f – noise models included in standard simulation tools are too simple and should be replaced by more accurate physics-based descriptions which are under development. At the beginning of this work, a unified noise model, either empirical or physical, that can predict the noise power in all bias regions had not yet emerged. However, it has been recently reported that flicker noise extensions of BSIM3 model with correlated terms [46] can fit all data in all bias regions but as it would be shown in chapter 4 that these models are also not consistent. No systematic method for managing 1/f noise has been established yet.

CHAPTER 4

FLICKER NOISE CHARACTERIZATION AND MANAGEMENT

4.1 1/F noise modeling issues

Although many investigations have been performed focusing on modeling the 1/f noise in MOS transistors, no definitive theory has been set forth to accurately explain the diverse results observed with real devices in the laboratories. A universally accepted model explaining the 1/f noise in p and n-channel MOS transistors is still lacking.

4.1.1 Flicker noise dependencies ("what appears to be known")

Bias dependence: There are controversies over the bias dependence of flicker noise as is evidence from the survey of 1/f noise models provided in the previous chapter. Bias dependence is likely associated with technology and operation region. It has been reported that it is possible to have bias dependent 1/f noise in one technology but no bias dependence in another [12,32].

Gate referred noise in NMOS has been reported to be independent of the bias point, both in the triode region and saturation region of operation [29,33] due to carrier density fluctuation. The input referred noise in PMOS has been reported to have a super linear gate voltage dependence due to mobility fluctuations in both linear and saturation region of operation [29]. Input referred noise in the subthreshold region has the same behavior as that in the strong inversion i.e. no gate bias dependence for n-MOSFETs [35]. The input referred noise decreases in magnitude as the device bias is varied from subthreshold into strong inversion for p-MOSFETs, which is very different from n-MOSFETs [35].

***Our observations based on small samples*:** K_f (flicker noise co-efficient) versus V_{ds} plot is shown in figure 4.1 for a particular device size for both NMOS & PMOS case.

The model we use for finding K_f is,

$$FNP = \frac{K_f I_D}{L_{eff}^2 f} \tag{1}$$

where $L_{eff} = L_{Si} - LR - TLD$, LR = Mask tolerance length reduction, TLD = Total lateral diffusion of source and drain, FNP = Flicker noise power.

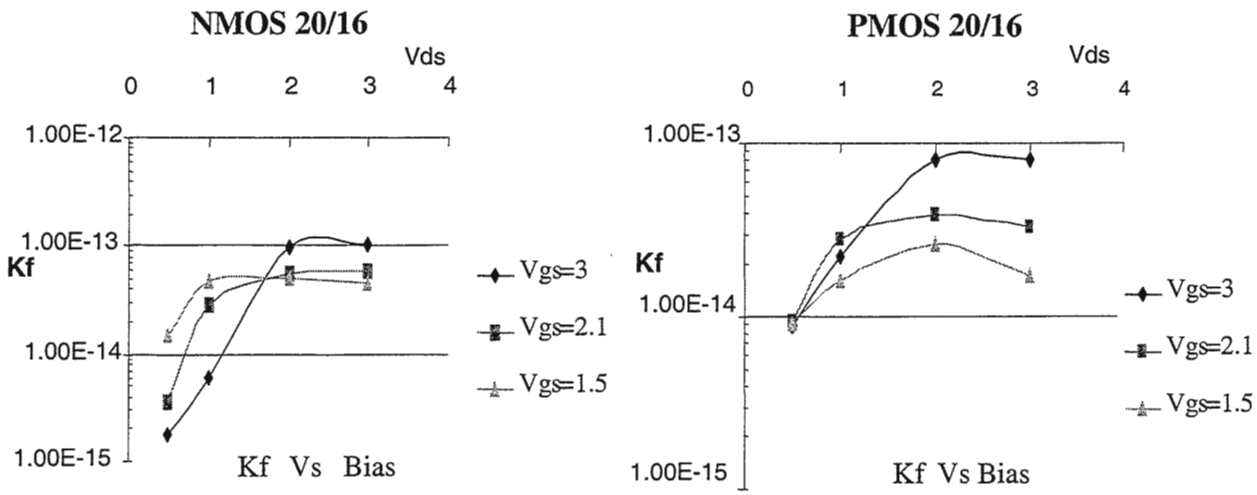


Figure 4.1 - Bias dependence of NMOS & PMOS devices

Fabrication and measurements of the devices were carried out at Texas Instruments, Dallas. From this particular data we can say that there is one to two order of magnitude of difference in K_f from linear to saturation region. K_f seems V_{ds} dependent in triode region where as, it seems V_{ds} independent in saturation region for both PMOS & NMOS devices. Our observation of K_f increasing linearly in triode region is also supported by very recent measurements published in literature [31]. K_f seems V_{gs} dependent in saturation region and it is possibly V_{gs} dependent in triode region too. As expected, p-channel device K_f is one order of magnitude lower than n-channel device. We will give more rigorous measurement data in

chapter 7 after measurements of test structures.

Device dimension dependence: Gate referred flicker noise has been reported inversely proportional to gate area (WL) [8,10,30]. For super-micron (L>1μ) MOSFETs flicker noise has been reported proportional to 1/L and it has been shown even stronger dependence on L for sub-micron MOSFETs [31].

Process dependence:

***Gate oxide thickness dependence*:** Beside changes in processing steps, which are inevitable, the downscaling of the technology has some fundamental consequences for the flicker noise. Traditionally (t_{ox} > > 100A°) noise performance improves as we scale down the oxide thickness [8,32] however, for deep submicron devices it is other way round [5].

Gate dielectric dependence: MOS devices with a gate dielectric other than silicon dioxide, such as nitrided films have been reported to have very different low-frequency characteristics. The frequency index γ of the noise spectrum ($\propto f^{-\gamma}$) has been shown to vary between 0.8 to 1.4 with the gate bias. A detailed analysis can be found in [5,33].

***Hot carrier stress dependence [34]*:** High electric fields present in short channel devices near the drain produce hot carriers in that vicinity for sufficiently large V_{DS} values. Hot-electron injection is known to cause degradations in transconductance, threshold voltage, drain current and is reported to cause an increase in 1/f noise in MOSFETs. Hot carrier stressing of n-channel MOSFETs can result in a tremendous (one to two orders) increase of flicker noise, whereas for p-MOSFETs the noise is hardly affected [29]. Degradations of the device characteristics due to hot-electron stresses arise mainly from the generation of electron-hole pairs at the drain end due to covalent bond breaking in this region, with some of the excess majority carriers ending up in traps at the Si-SiO_2 interface and deeper into oxide.

Other process parameters: Flicker noise depends on physical conditions during growing, doping, intentional & unintentional surface treatment and contacting.

Environment Dependence:

Temperature dependence [35]: Device type dependence and temperature dependence are shown to be correlated [18]. The n-MOS input referred noise spectra shows no bias dependence at all temperatures i.e. noise varies weakly with T. This gives credence to a tunneling model such as carrier density fluctuation, which is independent of temperature to a first order. The p-MOS input referred noise spectra shows gate bias dependence at all temperatures down to 5 K and can be conveniently modeled as a mobility fluctuation [26].

4.1.2 Positional Dependencies

The issue of the effects of device layout on 1/f noise characteristics has not been studied. In a conventional rectangular transistor, the channel region is not physically homogenous. The impurity profile near the drain and source differs from that in the center of the channel. Some consideration of this dependency was made in the studies of hot carrier stress. Correspondingly, along the edges of the channel, field oxide encroaches on the channel region causing a continual tapering of the channel until it disappears completely under the thick field oxide layer. This is known as the "bird's beaking" region[36,37,38]. The effects of the "bird's beaking" region on 1/f noise has not been studied. If there is a dependence different than that in the channel, devices with a large amount of bird's beaking (multiple parallel transistors) or devices with no bird's beaking (circular or concentric transistors) could be used to optimize the 1/f noise performance of the overall device. The "bird's beaking" region is discussed in the following section.

Device geometry dependence: Does circular transistor have less 1/f noise than rectangular?

4.2 Bird's Beaking

4.2.1 Theory of bird's beaking in rectangular devices

The width of a standard rectangular transistor is defined by the width of the active (channel) region and this width is terminated on both sides of the channel by field oxide.

During the field oxide growth, encroachment into the active region effectively reduces the drawn width W of a transistor. Effective width is obtained by the equation, $W_{eff} = W - 2\Delta W$, where ΔW is the encroachment of the field oxide on each side of the channel. This oxide encroachment is termed bird's beaking due to the shape of the encroachment under the gate oxide mask. This is troublesome because the width of the transistor is no longer precisely defined and because the exact amount of width reduction is not easily controllable. A top view of a normal rectangular transistor is shown in Figure 4.2.

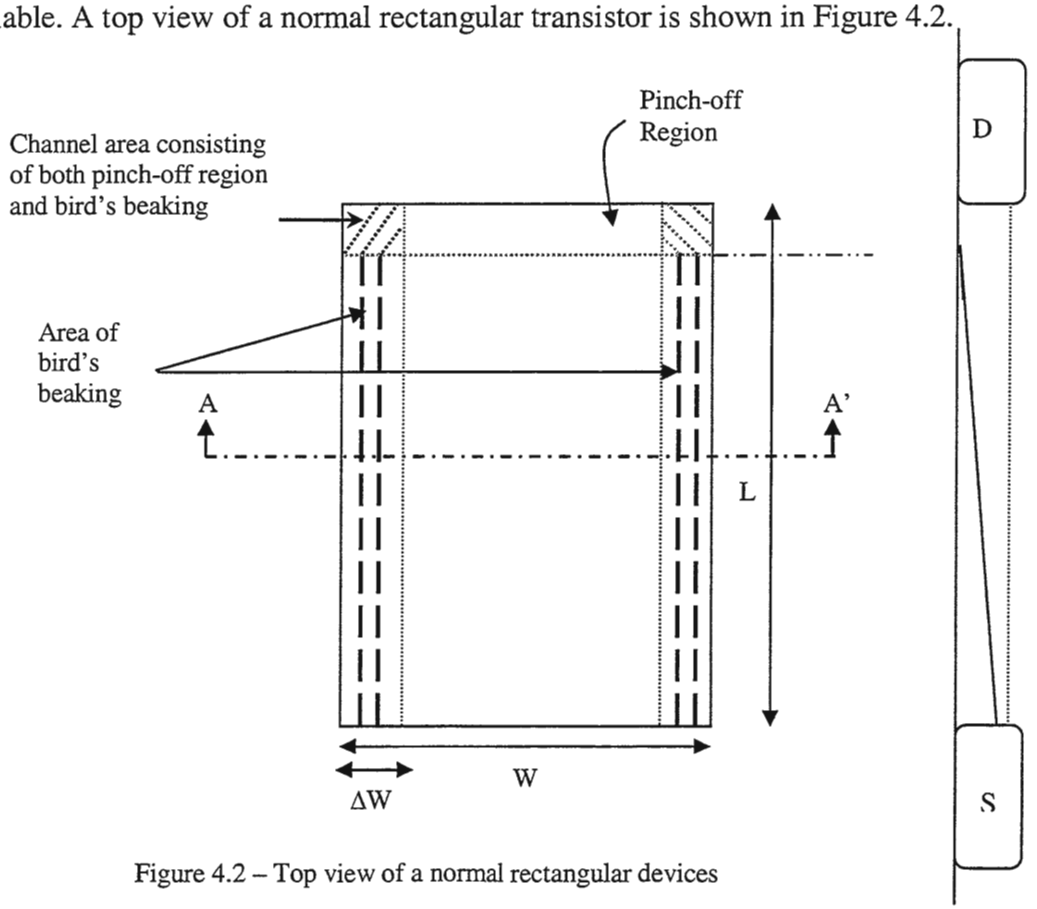


Figure 4.2 – Top view of a normal rectangular devices

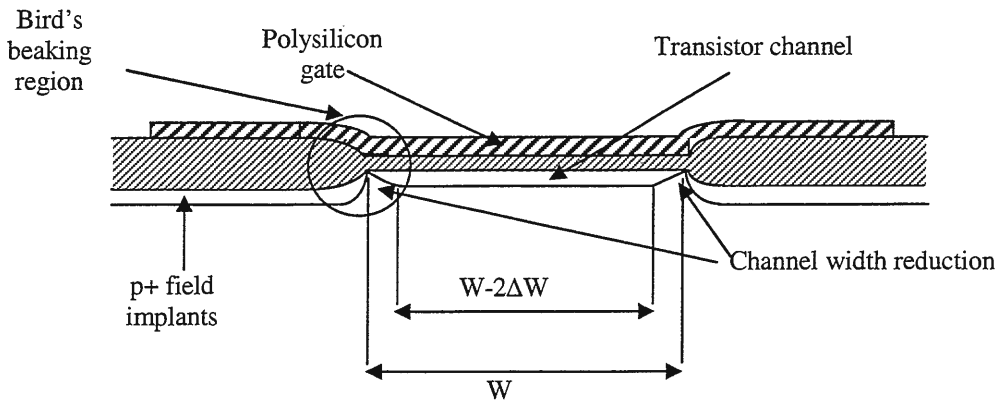


Figure 4.3 - The cross section AA' showing bird's beaking

The cross section of the device of Figure 4.2 along section AA' is shown in Figure 4.3. The p+ field implant under the field oxide causes the effective substrate doping to be greater at the sides of the transistors than elsewhere. This increased doping along with the increased gate oxide thickness in the bird's beaking region raises the effective transistor threshold voltage near the sides of the transistors and therefore decreases the channel-charge density at the edges. The result is that the effective width of the transistor is less than the width drawn on the layout mask. The effective width of the device is now W - 2ΔW.

Hypothesis on 1/f noise in bird's beaking region: As the device dimensions continue to shrink with each new generation of MOS technology, the role of individual defects on device performance becomes more pronounced. It is well recognized that MOS devices which form channels near the surface of a doped silicon region adjacent to a SiO_2 interface experience poorer 1/f noise performance than buried channel devices in which the major current flow path is restricted by reverse-biased p-n junctions. As feature sizes continue to shrink, there is concern that the percentage of the total channel current that flows near the surface in the bird's beaking region will increase. In the past, most of the work on 1/f noise in MOSFETs published in the literature has focused on the effects of oxide traps near the interface, but no

attention had been paid to the bird's beaking region which has a different interface with the SiO_2. ***Our conjecture is that 1/f noise is different in and likely worse in the bird's beaking region of a MOS transistor than it is in the homogeneous part of the channel.*** We will evaluate 1/f noise performance of MOS transistor with normal bird's beaking, with enhanced bird's beaking and with no bird's beaking. Particular emphasis will be focused on determining how K_f (flicker noise co-efficient) for the bird's beaking region compares with that for the other homogeneous part of the channel.

Typically, designers utilize the rectangular-shaped gate whenever possible since the rectangular geometry is convenient for layout, component density can be high and good models for this device have been developed. Nonrectangular devices (e.g. circular, concentric, trapezoidal, toroidal, 'V' shaped etc.) are occasionally used, however. A circular transistor is shown in Figure 4.4. It is apparent that this device has no bird's beaking region.

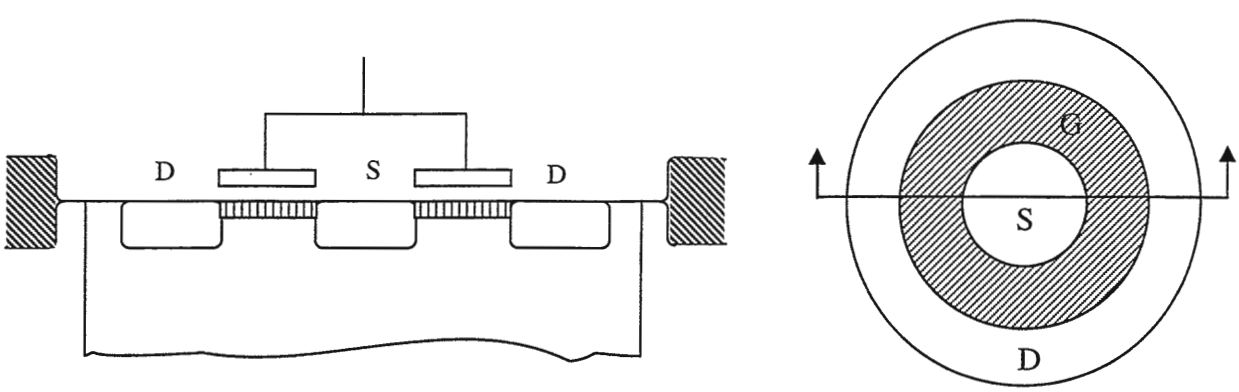


Figure 4.4 - Circular transistor (a) cross section (no bird's beaking) (b) top view

Correspondingly, layout can be used to enhance the bird's beaking region. Figure 4.5 shows two layouts of a wide rectangular transistor that ideally both have the same effective length and width. The layout on the right is a segmented layout. The segmented layout has n times as much bird's beaking region where n is the number of segments.

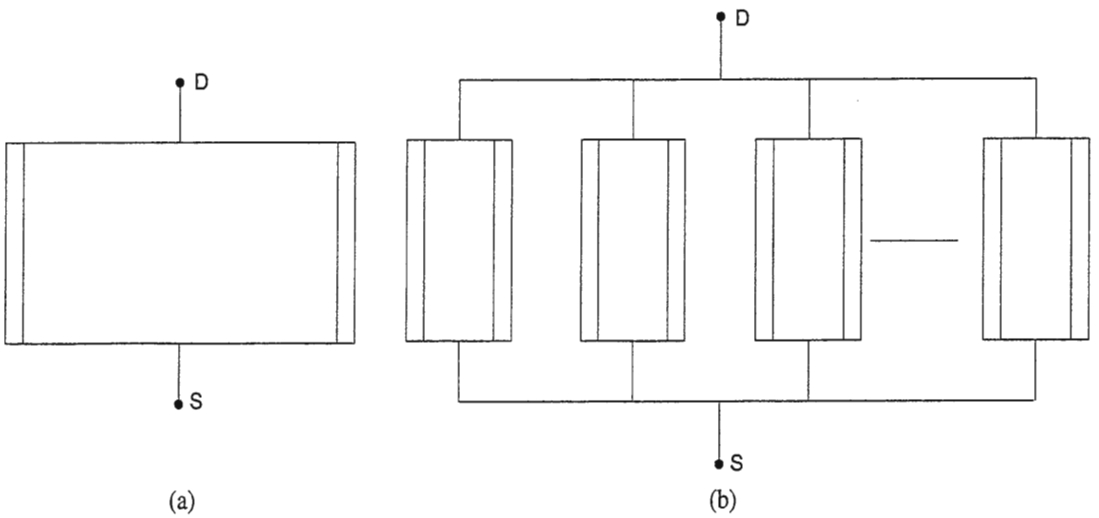


Figure 4.5 - Layout for enhancing the bird's beaking region (a) Conventional (b) Segmented

4.2.2 Literature references

It has been reported very recently [39,40] that some type of RTS noise (see chapter 3.2.3 – Random telegraph noise) may be related to the isolation edges of the device. In other words, it could originate from the bird's beak regions of the surrounding thicker isolation oxides, close to source and the drain. One argument in favor of this is the observation that the RTS-signals do not disappear when the device is measured in the gated source or drain diode configuration. However, more work is necessary to establish the role of the device isolation on the low frequency noise and RTS behavior in submicron MOSFETs [39,40]. These two papers [39,40] are the only papers published in the literature so far according to our knowledge and they predict flicker noise mechanism as RTS phenomenon.

4.3 Inconsistency in existing models

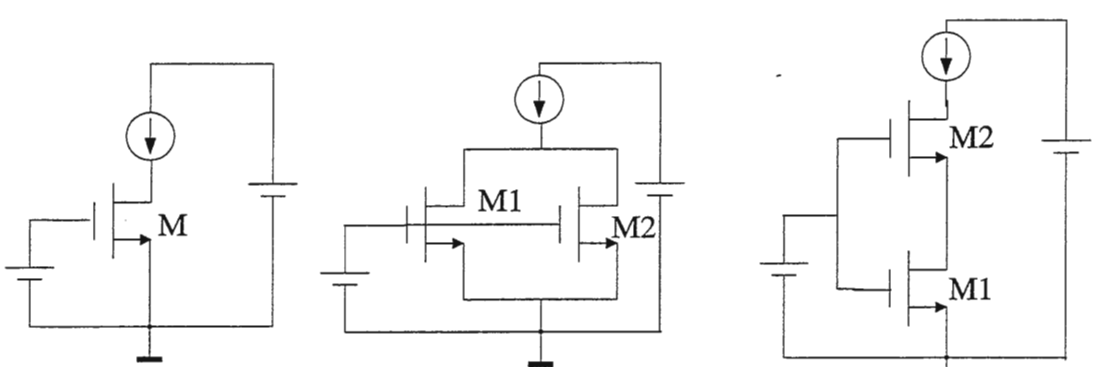
Thermal noise models: Table 4.1 shows the results of HSPICE level 49 simulations for thermal noise for series and parallel connections of two transistors for NLEV=0 and NLEV=3 in a 0.35u CMOS process. The circuit used for the simulation is shown in Figure

4.6 The models used in HSPICE are given in [16].

In these simulations, the drain current varies slightly in the various representations because of ΔL and ΔW effects. These variations indicate that alternate representations are not quite the same but sufficiently close that we would expect the 1/f noise currents to be very close. As can be seen, the noise currents vary significantly. The condition becomes even worse when more than two (say ten or twenty) transistors are connected in series or parallel combinations. It is apparent from these simulations that simple thermal noise model (8/3 kTgm) equations are inconsistent because they don't predict the triode region noise very well. In fact, Wang et. al. [47] presented the model which is capable of predicting both triode and saturation region thermal noise very well for short and long channel devices. For BSIM3v3 [36] thermal noise model is

$$S_I = \frac{4kT\mu_{eff}}{L_{eff}^2}|Q_{inv}| \qquad (2)$$

where Q_{inv} is the inversion channel charge computed from the capacitance models. We verify the results with simulations as given in Table 4.2.



(a) W/L

(b) (W/2)/L each

(c) W/(L/2) each

Figure 4.6 - Test circuits for thermal and 1/f noise simulations

Table 4.1 - HPSICE Level 49 simulations for thermal noise (inconsistent model)

Configuration	Vds (V)	Vgs (V)	Ids (uA)	Total Output thermal noise V/√Hz (NLEV=0)	% Variation	Total Output thermal noise V^2/Hz (NLEV=3)	% Variation
Single transistor 5/20	10.03	3	89.1	4.121E-06		4.773E-06	
Two parallel transistors 2.5/20 each	10.23	3	85.6	4.204E-06	2.01%	4.921E-06	3.11%
Two series transistors M2 5/10 each M1	9.52 0.637	2.36 3	87 87	3.764E-06	-8.65%	6.368E-06	33.42%
Two series transistors, M2 top 5/15, bottom 5/5 M1	9.93 0.3	2.7 3	87.5 87.5	3.808E-06	-7.59%	5.433E-06	13.84%
Two series transistors M2 top 5/5, bottom 5/15 M1	9.258 1.062	1.94 3	86.2 86.2	4.913E-06	19.23%	8.562E-06	79.38%

Table 4.2 – BSIM3v3 simulations for thermal noise (consistent model)

Device	Vgs (V)	Vds (V)	Ids (A)	Total Ouput Thermal noise (V/√Hz)	% Variation	Operating Condition	Comment
100/30	1	3	5.125E-06	2.478E-05		Saturation	BSIM3 Model
100/15 100/15	0.931 1	2.931 0.069	5.331E-06 5.331E-06	2.603E-05	5.04%	Saturation Triode	BSIM3 Model
100/10 100/20	0.958 1	2.958 0.0425	5.270E-06 5.270E-06	2.540E-05	2.51%	Saturation Triode	BSIM3 Model
100/20 100/10	0.897 1	2.897 0.103	5.353E-06 5.353E-06	2.626E-05	5.96%	Saturation Triode	BSIM3 Model

Flicker noise (1/f) models: Table 4.3 shows 1/f noise simulation results for single big transistor, two transistors in series and with different combinations of two transistors such that effective W/L is same as discussed in chapter 2 in detail. Noise model used for this analysis is given in equation (3) of chapter 3 which is the most widely used model. Because this model cannot predict triode region 1/f noise accurately, it overestimates the overall noise

Table 4.3 - Simulation showing gross inconsistency in Spice2 model for 1/f noise

Device	Vgs (V)	Vds (V)	Ids (A)	Total Ouput 1/f noise @ 10 Hz (V/√Hz)	% Variation	Operating Condition	Comment
100/30	1	3	5.125E-06	1.8709E-04		Saturation	Spice2 model
100/15 100/15	0.931 1	2.931 0.069	5.331E-06 5.331E-06	2.9496E-04	57.66%	Saturation Triode	Spice2 model
100/10 100/20	0.958 1	2.958 0.0425	5.270E-06 5.270E-06	2.8095E-04	50.17%	Saturation Triode	Spice2 model
100/20 100/10	0.897 1	2.897 0.103	5.353E-06 5.353E-06	3.0113E-04	60.95%	Saturation Triode	Spice2 model

of the two devices in series as shown in the Table 4.3 by 50 to 60 percent even for two transistor case. Noise estimates get poorer as we increase number of devices in series because only the top device is in saturation where rest all are in triode region of operation. None of the models used in the industry or in academia predict the 1/f noise in triode region accurately. Berkeley BSIM3 two term model (equation 8.2 in [46]) which takes into account the bias dependence is supposed to have better prediction for 1/f noise in triode region. This model has been very recently being used by the industry people. 1/f noise simulations for this model are shown in Table 4.4.

Table 4.4 – 1/f noise simulation with Berkeley 2 term model (inconsistent model)

Device	Vgs (V)	Vds (V)	Ids (A)	Total Ouput 1/f noise @ 10 Hz (V/√Hz)	% Variation	Operating Condition	Comment
100/30	1	3	8.124E-06	2.43E-04		Saturation	2 Term Berkeley model
100/15 100/15	0.923 1	2.923 0.076	8.504E-06 8.504E-06	3.55E-04	45.72%	Saturation Triode	2 Term Berkeley model
100/10 100/20	0.886 1	2.886 0.114	8.551E-06 8.551E-06	4.38E-04	79.82%	Saturation Triode	2 Term Berkeley model
100/20 100/10	0.953 1	2.953 0.047	8.408E-06 8.408E-06	3.01E-04	23.48%	Saturation Triode	2 Term Berkeley model

As we can see from the Table 4.4 that even BSIM3 model for 1/f noise is inconsistent, however, it is a first step towards the solution. We would show later on in chapter 7 by huge number of measurements that it's essential to have separate K_f for triode region of operation. Flicker noise coefficient is strongly bias dependent which most of the existing widely used models don't take into account.

Table 4.5 shows simulation results for single 32/8 device and two 32/4 devices in series. As we see from the table, spice2 model (equation (3) of chapter 3), is 31% off from the single transistor. We introduced a new model here by actually taking the K_f from the actual measurement at that particular bias point and incorporating it for the lower device of

Table 4.5 – Consistency in series connected devices using different K_f for linear and saturation region transistors

Device	Vgs (V)	Vds (V)	Ids (A)	Total Ouput 1/f noise @ 10 Hz (V/√Hz)	% Variation	Operating Condition	Comment
32/8	2	3	143.4E-6	5.6723E-05		Saturation	Spice2 Model
32/4 32/4	1.609 2	2.6 0.39	143.4E-6 143.4E-6	7.4460E-05	31.27%	Saturation Triode	Spice2 Model
32/4 32/4	1.609 2	2.6 0.39	143.4E-6 143.4E-6	5.8970E-05	3.96%	Saturation Triode	Spice2 Sat Kf, & Measured Triode Kf

the two series connected devices. By actually taking into account the bias point of the triode region device and using the premeasured K_f for that particular bias point gave us pretty accurate noise prediction of the two series connected devices. Thus, we have shown here that better model is required which can predict the triode region noise more accurately and by doing that we can get a consistent noise model.

CHAPTER 5

FLICKER NOISE MEASUREMENT

5.1 Challenges with noise measurement

The accurate measurement of fluctuation phenomena, or noise, in semiconductor devices is a problem of great interest, in part, because this determines the minimum resolvable signal in amplifiers, the jitter in oscillators and also provides insight into fundamental properties of semiconductor materials and device behavior [44]. Due to the importance of noise in analog and mixed signal applications, accurate noise measurement warrants our careful attention. Properly collected noise data is a key parameter which is often "behind the scenes". Several types of noise are of concern. In this thesis, emphasis will be placed on a single type of noise, flicker noise. Flicker noise measurement is often a complicated and time-consuming process.

5.2 Basic setup

Noise signals are generally quite small making it difficult to accurately measure noise with general purpose test equipment. To overcome this problem, noise measurements are usually performed by following the Device Under Test (DUT) with an amplifier whose noise is less than that of the DUT. The amplifier is used to sufficiently enhance the magnitude of the noise of interest so that it may be read on a spectrum analyzer or some other narrow-band power meter [10,26,41,42].

The measurement setup for our system is shown in Figure 5.1. The noise current that is to be measured is modeled by the noise current source $\bar{i}_n^2$. The noise amplifier is a high gain transresistance amplifier. In this method, the noise current in the FET channel is passed

through the resistor to generate a noise voltage that is proportional to the noise current. This voltage is then amplified by the noise voltage amplifier and measured by a Dynamic Signal Analyzer (DSA). To resolve the noise of interest, it is essential that the noise current of the load resistor be less than the FET noise which requires the internal resistor R_L to be large.

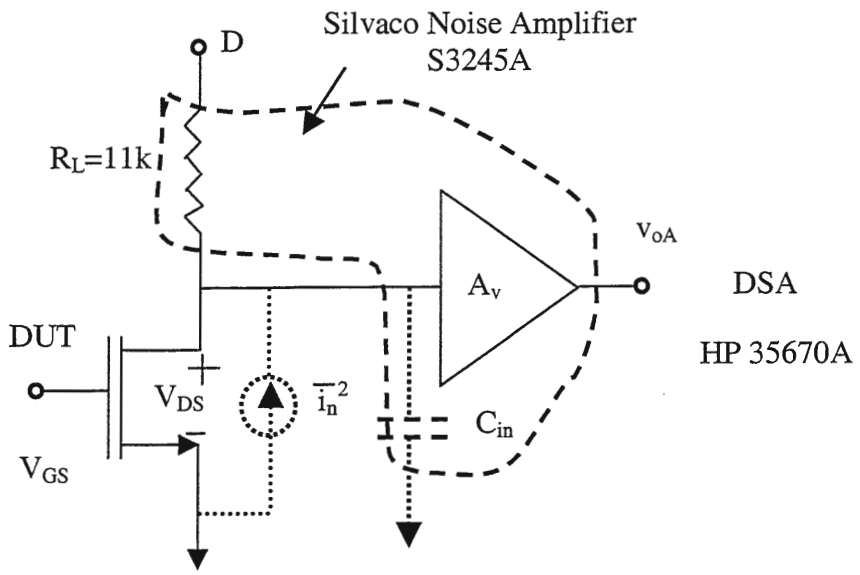


Figure 5.1 - Setup diagram for noise measurement

The frequency response of the system is determined by R_L and the capacitances to the amplifier input and parasitics C_{in}.

In our measurement system, the amplifier we used is a Silvaco S3245A noise amplifier [43] which has a voltage gain of A_v=121 for frequencies up to 84 kHz. It has an internal impedance of 11k. A computer controlled test system has been developed to conduct the I-V and noise measurements. A shielded Cascade Microtech general-purpose probe station with a low noise chuck was used to characterize devices at room temperature. The gate and drain biases are provided by a Hewlett Packard HP4142 stimulus and measurement units (SMUs). The residual noise in the bias sources is minimized by RC filters internal to

the noise amplifier. The amplified signal denoted as v_{oA} is fed into a Hewlett Packard HP35670A Dynamic Signal Analyzer (DSA). It computes the fast Fourier transform of the noise signal and averages the calculated power spectra over twenty measurement cycles to smooth the spectrum. The averaging feature of the DSA combines each newly measured spectrum point with previous data on a point-by-point basis using a standard root mean square calculation. The measurements were made at the wafer probe level. System (parasitic/background) noise measurements were made at every single measurement and the resultant background noise was subtracted from each measurement. Some preliminary measurements were made by measuring the background noise only at the start of a test and then subtracting this noise from all measurements. The former method resulted in repeatable measurements which could not be achieved by making a single background noise measurement. All noise measurements were made in a device characterization laboratory at Texas Instruments Inc. The Texas Instruments internal software environment provided for GP-IB control, a user friendly windows environment, automatic and simplified data acquisition, and analysis for wafer-level device measurements. It also has a built in optimizer. The frequency range under study is 1 to 100Hz.

5.3 K_f (Flicker noise co-efficient) measurement procedure

A two step approach will be used for the measurement of noise model parameters. First, the noise spectral density S_N will be measured over the frequency range of interest. Following this measurement, the model parameters will be extracted. As was observed in chapter 2, there is some level of inconsistency in all 1/f noise models that have appeared in the literature. The measurement of S_N is not impacted by these inconsistencies. The

extraction of the noise model parameters is strongly dependent upon the functional form of the noise model.

The measurement setup described in the previous section will ideally measure all of the noise present throughout the measurement band. Since we are only interested in the 1/f noise characteristics, we will limit that frequency band to that where the 1/f noise is dominant and make the assumption that the contribution of all other noise sources are negligible; i.e. we will assume the measured noise is the 1/f noise. In almost all current MOS devices, the 1/f noise mechanisms are dominant at frequency below 100 Hz. For this mean, we will take S_N measurements in the two decade band from 1 Hz to 100 Hz.

We will assume that the 1/f noise is modeled by the equation,

$$S_{N,TRIODE} = S_{N,SAT} = \frac{K_F I_{ds}}{L_{eff}^2 f^{AF}} \tag{1}$$

where K_F and AF are constants, I_d is the quiescent drain current and L_{eff} is the effective gate length. From the spectral density measurements, we will extract the parameters K_F and AF.

Define S_N to be the noise current spectral density of the DUT. If S_{NO} is the spectral density at the output of the noise amplifier, S_{BO} is the spectral density at the output of the noise amplifier without the DUT in the circuit, g_{ds} is the small signal output impedance of the DUT. It follows from a routine calculation that

$$S_N = \frac{(S_{NO} - S_{BO})(1 + g_{ds} R_L)^2}{A_v^2 \bullet R_L^2} \tag{2}$$

where A_v is the voltage gain of the amplifier.

Although not evident from (1), the spectral density is dependent upon operating point in addition to device size. For this reason, a single parameter K_f that is characteristic of the

process does not exist. As a consequence, we will measure the spectral densities at several operating points in different region of operation for several different sized devices.

Several issues relating to the measurement of S_N deserve mention:

(1) Make sure you don't exceed the voltage limitations of the process at any given time.

(2) g_{ds} at the bias point should be measured rather than calculated to minimize error in associated with model for g_{ds}.

(3) Background noise can vary from time to time and hence should be measured at every measurement of S_N.

A typical comparison of system noise and system plus device noise at the output of amplifier is shown in Figure 5.2.

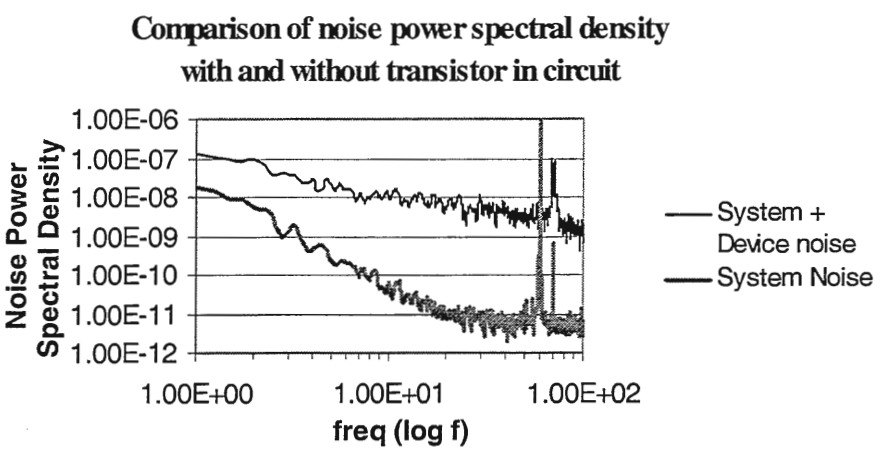


Figure 5.2 - Comparison of device plus system noise and system noise

Optimization of corrected data to extract K_f: Measured data contains spike at 60 Hz if AC power lines are used. This spike (and any other spike depending on environment) should be removed to extract K_f parameter for better accuracy. A typical K_f extraction plot is given in Figure 5.3. Figure 5.3 shows the plot of corrected flicker noise voltage spectral density

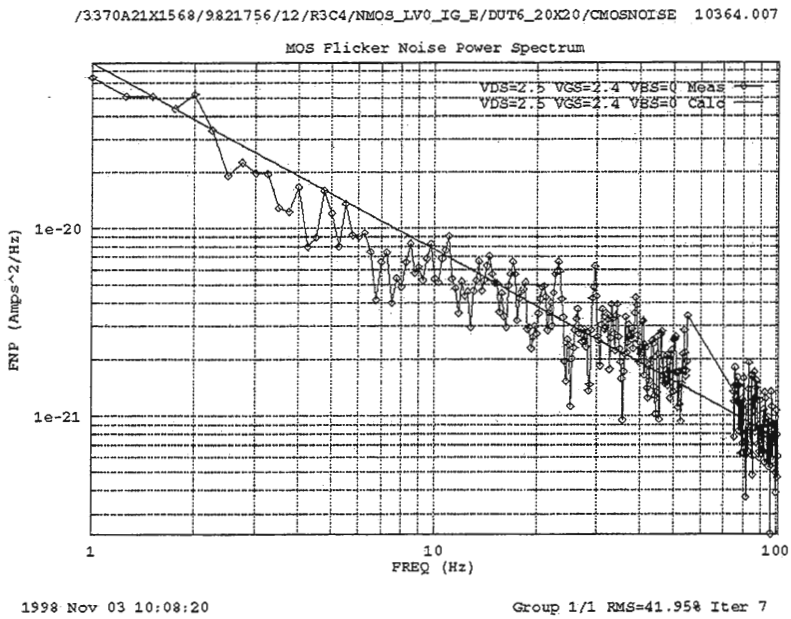


Figure 5.3 - Corrected and optimized drain current noise power(FNP) to extract K_f

versus frequency. Basically, it shows the device noise alone and the system noise is subtracted from the total noise measurement. Certain frequency components around 60 Hz are removed as shown in the plot with the help of internal software at Texas Instruments, Inc to give better accuracy. Equation (2) is then used to calculate equivalent drain referred current spectral density. A line y = a + bx is fitted to this corrected data with the following equation,

$$Error = \sum_{i=1}^{n} w_i \left(\overline{y} - (a + bx)\right)^2 \tag{3}$$

where weight w_i is assumed to be one. Intercept of this fitted line to the y-axis gives corrected flicker noise spectrum density S_N of equation (2). Finally Equation (1) is used to calculate flicker noise coefficient K_f with the assumption that AF=1. In fact, as we demonstrate in Chapter 7, these two assumptions of AF=1 and w_i=1 are the potential sources of errors and we demonstrate much better and improved algorithm to extract K_f in Chapter 7.

5.4 Precautions/guidelines to reduce ambient noise

In this section, we describe some general guidelines and "rules of thumb" to reduce ambient noise as well as to get better measurement accuracy. Since noise is a random process, there are no predefined rules to guarantee good measurement but we believe these guidelines could be very useful for those interested in making noise measurements.

- Since the noise levels being measured are low, the noise signals must be amplified through a low noise amplifier. It is much easier to get good measurements if the noise of the amplifier is lower noise of the device under test that appears at the output of the amplifier.
- Connecting cables should be at least double shielded co-axial cables to protect signal integrity from undesired interference of CRT monitors, computer CPUs and other measurement instruments. Preferably all cables should be short and of equal length. Precisely, the cables carrying AC signals (from DUT to noise amplifier) should be of good quality and properly shielded.
- It is very important to carry out good calibration of the measurement setup and the instruments being used. The measurement setup must give repeatable measurements. Developing a measurement environment that gives repeatable measurements of 1/f noise is one of the most challenging tasks in 1/f noise measurements. If a system does not give repeatable measurements, the measurement results will be in question and any resulting extracted parameters will be of limited or no use.
- Experience has shown that location of the setup plays one of the major roles in establishing a stable and repeatable system. Preferably the location of the setup should be in a corner of a room with minimal disruptions and changes in the environment. This

means minimal movement of equipment, furniture and people in the area. Only test equipment that is essential to the measurement should be powered in the vicinity of the DUT. Providing a separate screen room might be a good idea but it could be very expensive as well. Noise amplifier and dynamic signal analyzer should be kept at least 1-2 ft above ground level. Although there is no physical evidence but it is conjectured that low height ceiling and carpeted floor could play little part in establishing good system too.

- The device under test should be properly biased and shielded from parasitic noise sources. The probe station should be completely shielded. A low noise chuck will definitely help. Properly shielded manipulators play a major role in preserving signal integrity. Hours of time can be spent trying to maintain repeatability from the setup and instruments when there is a problem in the manipulators. Preferably manipulators should be shielded all the way up to the probe tips. Sometimes we find oscillations in DC and AC measurements; putting a ferrite bead on the manipulators of the gate terminal has helped solve this problem.
- Batteries should be chosen to power the DUT rather than the ac line power supplies in order to minimize external noise sources. However, care should be taken if battery has a nonzero output resistance. There should be a common ground for all instruments and single power strip should be used if possible. When using batteries, they should be routinely tested to verify that they are adequately charged. In this work, we had used HP 4142 SMU(Source and Measurement Unit)s which were powered by ac line supply.
- All ambient lights should be turned off if possible. Even though a probe station is optically shielded, we have experienced a difference in measurement because of ambient

lights. Additional light sources inside the probe station could cause charge injection. We have seen charge injection as high as 2-10 microamperes and hence those light sources should always be turned off during measurements.

- The noise floor of the measurement setup (background noise) must be measured before each device measurement. We found that doing the noise measurement immediately after the device noise measurement did not give repeatable results and is possibly due to charging-discharging of capacitors in the noise filters in the noise amplifier in our case.
- System noise is bias dependent in our case and we noticed that for the Silvaco Amplifier configuration which is used in the measurement, the system noise could change by as much as an order of magnitude depending on the V_{ds} of MOS transistor. It took ten days for us to figure out the system noise problem because of V_{ds} dependence of the Silvaco noise amplifier. So, bias conditions should be always specified when doing the noise measurement for good accuracy even though the DUT is disconnected from the circuit.
- While doing the device noise measurements, sufficient delay should be provided in order for noise amplifier to work properly. For example, if you are measuring noise at 1 Hz, it will take 1s for that 1/f noise event to occur. But, if you are measuring noise at 0.1 Hz, it will take 10s for that 1/f noise event to occur. In other words, sufficient delay should be provided for events to occur during measurements so that capacitors in the noise filters can charge and discharge completely. In our case, we were measuring 1/f noise spectrum from 1 Hz to 100 Hz and 10s delay was found sufficient for us.
- Gds of the device should be measured at every bias point, rather than calculated, for better accuracy.

- g_m (transconductance) of the device should be also measured at every bias point if you are measuring input referred noise.
- Nighttime has given us the best noise measurement data. Carefully taken data (reliable data) is the single most important thing in drawing any conclusion.
- Substrate leakage current can be a problem. We have noticed during our experiments that sometimes due to improper handling of the device during measurement causes ESD (Electro Static Discharge) mechanisms. Because of it, we noticed that it would result in either change of operating point and/or substantial change in substrate current. Substrate current should be monitored all the times. Damage to the device could occur if too high V_{gs} or V_{ds} is applied. Data taken on devices with substantial substrate leakage current (nano amperes) should be discarded.
- Guard rings, if used, should be properly biased.
- Since there are variations in process parameters from die to die, wafer to wafer and lot to lot, enough samples should be taken before making any solid conclusions. Bias conditions should be specified while specifying K_f.
- If measurement probe tips are not pushed hard enough to the pads there could be a open circuit condition in the circuit which results in errors in DC characteristics. Making the contacts properly solves the problem.
- The measurements of 1/f noise is a slow process. It took us approximately one month with 18-22 man hours/day to conduct all the experiments in the Linear BiCMOS LOCOS process to measure the noise in the frequency spectrum of 1-100Hz. We had taken more than 250 successful reliable measurements. It took us almost week to ten days to characterize the system for good repeatability. If we were to conduct the same

measurements in the frequency span of 0.1 Hz to 100Hz the time to complete the measurements would have been more than double.

CHAPTER 6

TEST STRUCTURES

Test structures were fabricated in two different processes at Texas Instruments, Dallas. The results provided in this thesis came from a Linear n-well BiCmos process that has SDD (Singly Doped Drain) devices. This process has a nominal oxide thickness of 425 A°, nominal V_T of 0.7V, and a maximum supply voltage Vdd of 5V. Minimum effective channel length for the devices is 2u and minimum width is 2.5u. PMOS transistors are not affected by SDD layer. All the test structures used in this thesis were also fabricated in a more advanced Shallow Trench Isolation (STI) n-well CMOS process[28]. In STI process, a "trench" filled with oxide isolates devices from one another; thereby allowing the devices to be packed closer to each other without compromising latchup immunity. This STI process has a gate oxide thickness of 35 A°, a maximum Vdd of 1.8V and it also has analog friendly low V_T device in addition to a higher V_T device. The minimum drawn channel length is 0.6um and the minimum effective channel length is 0.21um. Results in the STI process will not be discussed in detail in this thesis because the processing was not completed until after the bulk of this thesis was completed. Transistors in the test structures were individual devices without any input or output protection circuits. Guard rings were provided for all n- and p-channel structures.

6.1 Structures characterizing bird's beaking noise effects

Our main hypothesis is to test if the current in the bird's beaking region of the channel plays a different role in the 1/f noise of a device then current in the fully inverted

channel. So, our aim was to have structures with different percentage of bird's beaking to characterize the sidewall noise effects. The structures used for characterizing bird's beaking

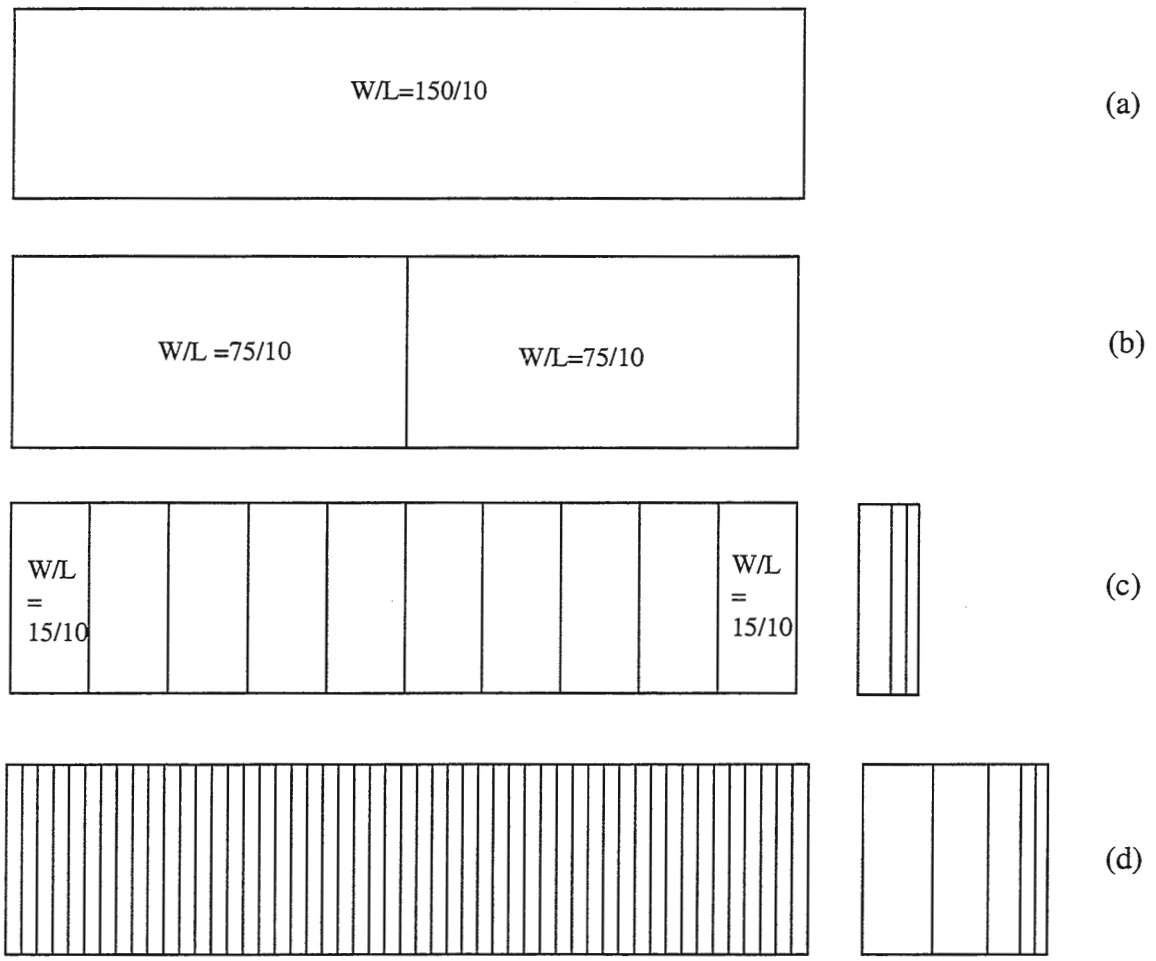


Figure 6.1 - Different structures to characterize bird's beaking noise effects

noise effects are shown in Figure 6.1. All structures were designed to have the same nominal W/L ratio but to have different amounts of bird's beaking. A discussion of each of the test devices follows.

Case (a) – 2 edges nominally: Normal rectangular transistor of size 150/10 (area of 1500 μ^2). Bird's beaking is a width effect and in this structure ΔW reduction will be along the two

edges. Total width reduction is negligible compared to overall width. This structure has the smallest amount of bird's beaking of the four test structures.

Case (b) – 4 edges nominally: Figure 6.1 (b) shows two transistors of W/L=75/10 each in parallel and hence effective W/L=150/10 which is same as Fig 6.1 (a). ΔW reduction will be along the four edges in this structure and so it is doubled than case (a). It has twice as much bird's beaking area as the previous structure.

Case (c) – 20 edges nominally: Figure 6.1 (c) shows ten transistors of W/L=15/10 each in parallel. As shown in Figure 4.2 and explained in Section 4.2.1 in Chapter 4, bird's beaking effectively reduces the width of the transistor. So, connecting ten transistors in parallel of 15/10 each will not give same effective W/L=150/10 as before.

For 10 transistors in parallel, 20 edges need to be compensated for width reduction (Since single transistor will have 2 edges for width reduction) to keep the effective W/L ratio equal to that of the simple layout of Figure 6.1 (a). For this process, the worst case width reduction is specified as,

Wint = 0.5048μ (worst case width reduction parameter from strong, nominal and weak models). Thus the worst case width reduction of the ten parallel transistors is

Winteq = 20*0.5048μ = 10.096μ.

This is 6.73 % of the nominal transistor width. To compensate for this reduction in the effective width, additional transistors with dimensions of W/L=8/10(5.33%), 4/10(2.66%), 2.5/10(1.66%) were placed in parallel with the original devices so that they can be laser trimmed to match the effective W/L ratio to that of the device of Figure 6.1 (a). The combination of additional transistors is provided such a way that the effective W/L ratio can be matched with an accuracy better than 1-2%. We will laser trim the additional devices after

comparing the DC current of this structure with the one in figure 6.1 (a). Compensation for width reduction is the same for both N & P devices. It should be noted that the number of edges will be increased from 20 to 22-24-26 depending upon how much trimming is required.

Case (d) – 100 edges nominally: Figure 6.1 (d) shows fifty transistors of W/L = 3/10 each in parallel. This structure will have even more width reduction (due to high bird's beaking area) since now 50 transistors are connected in parallel. The worse case width reduction for this structure is

Winteq = 100*0.5048μ = 50.48μ

This corresponds to a worst case reduction of the effective W/L ratio of 34%. We can see that this is a very significant number. To compensate for this W/L ratio reduction, we included additional transistors of W/L=32/10(21.33%), 16/10(10.66%), 8/10(5.33%), 4/10(2.66%), 2.5/10(1.66%). As before, the appropriate combination can be chosen with a laser trimmer. Compensation is the same for both N & P devices. This structure has a total bird's beaking area that is over 50 times as large as that of Figure 6.1 (a).

6.2 Structures characterizing geometry and bird's beaking noise effects

Typically, designers utilize the rectangular-shaped gate whenever possible since the rectangular geometry is convenient for layout, component density can be high and good models for this device have been developed. Nonrectangular devices (e.g. circular, concentric, trapezoidal, toroidal, 'V' shaped etc.) are occasionally used, however. Here we have two non-rectangular test structures to study the flicker noise difference between rectangular, circular and concentric devices. These two non-rectangular test structures have been selected because they have no bird's beaking region. Typically analog designers don't

use minimum channel length devices and hence the test structures we have used to characterize geometry and bird's beaking effects on 1/f noise are also big devices. Both the circular and concentric devices were designed to have the same effective W/L ratio and area as their rectangular counterpart.

6.2.1 Mapping between circular and rectangular transistors with the same effective W/L ratio and equal area

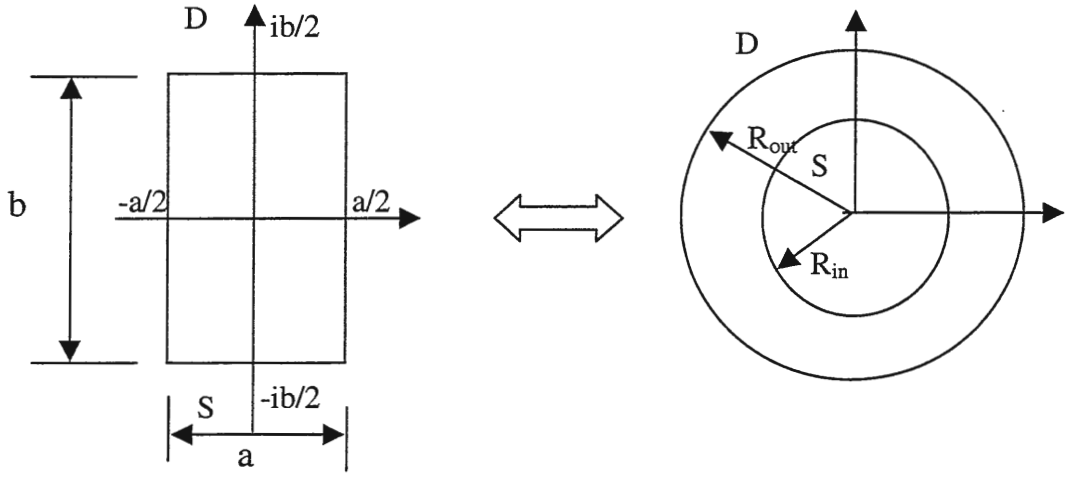


Figure 6.2 - Mapping between circular and rectangular transistor

A circular transistor is shown along with a rectangular transistor in Figure 6.2. For circular transistor [44], the equivalent W/L is given by the expression,

$$\left(\frac{W}{L}\right)_{eq} = \frac{2\pi}{\ln\left(\frac{R_{out}}{R_{in}}\right)} \tag{1}$$

The equivalent W/L ratio for the rectangular transistor is

$$\frac{W}{L} = \frac{a}{b} \tag{2}$$

The active area of circular transistors is given by,

$$A_{circ} = \pi (R_{out}^2 - R_{in}^2) \tag{3}$$

The active area of rectangular transistors is given by,

$$A_{rect} = ab \tag{4}$$

To have same area in both cases,

$$ab = \pi (R_{out}^2 - R_{in}^2) \tag{5}$$

From (1) and (2),

$$R_{out} = R_{in} e^{\frac{2\pi b}{a}} \tag{6}$$

Solving (5) and (6) simultaneously we obtain,

$$R_{in} = \sqrt{\frac{ab}{\pi\left(e^{\frac{4\pi b}{a}} - 1\right)}} \tag{7}$$

and

$$R_{out} = e^{\frac{2\pi b}{a}} \sqrt{\frac{ab}{\pi\left(e^{\frac{4\pi b}{a}} - 1\right)}} \tag{8}$$

Equation (7) and (8) give the equivalent R_{out} and R_{in} of the circular transistor required to have the same effective W/L ratio and area as the rectangular device. Note that although the circular transistor does not have a bird's beaking region, the current density in the channel is not uniform unlike that of the rectangular device where the current density in the channel is uniform.

6.2.2 Mapping between concentric and rectangular transistors with the same effective W/L ratio and equal area

A concentric device is shown in the Figure 6.2. Similar to circular devices, concentric devices do not have a bird's beaking and also have non-uniform current density in the channel.

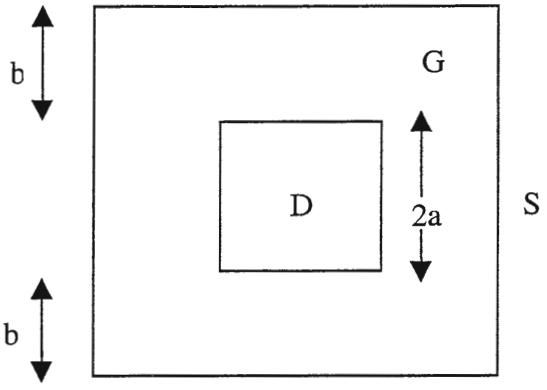


Figure 6.2 - Concentric device (no bird's beaking)

From [44], the equivalent W/L ratio for the concentric structure is given by,

$$\left(\frac{W}{L}\right)_{eq} = 4\left(\frac{2a}{b} - 7x10^{-5}\alpha^2 + 1.57x10^{-2}\alpha - 2x10^{-3}\right)_{\alpha = 45°} \quad (9)$$

The area of the complete structure is given by,

$$A_{conc} = (2a + 2b)^2 - (2a)^2 \quad (10)$$

For a given W/L of a rectangular device and to get the same area for concentric and rectangular cases we can equate areas and solve simultaneous equations (2), (4), (9) and (10) to get desired values.

6.3 Other structures

Apart from all the structures discussed above, we also have the following structures:

Structures characterizing series connected devices: We have different structures with one, two, ten and twenty devices in series and all of them with the same effective W/L. For ten and twenty devices in series configuration, the top device will be in saturation and the rest all

will be in the linear region. Since there are number of devices in series, the overall lateral diffusion becomes significant. We have added laser trimmable structures to compensate for this length reduction in the ten and twenty devices in series configuration. The laser trimmable structures have metal links which allow for the removal of the trimming devices. These extra devices are included so that we can trim to attain the same effective W/L. As explained in Section 2.2.2, a consistent noise model should have the same noise for any number of devices in series provided the same effective W/L ratio and same operating point is maintained.

Structures characterizing width and length effects: We have different structures characterizing width effects, length effects. Basically there are group of structures where one parameter (width or length) is kept constant and other parameter (length or width) would be varying. Non-varying parameter is kept much larger than minimum size in order to have no first order effects.

Structures characterizing operating region and bias dependence: Any of the available structures could be used to verify operating region and bias dependence of flicker noise.

Structure verifying shadow effects: Traditionally, during the implantation of the drain and source, the channel part is covered by the protection layer (e.g. SiO_2, Si_3N_4 etc). A tilt angle of about 7° is used between the incident ion-beam and the normal of the wafer surface. This is to avoid deep penetration of the ions due to a channeling mechanism. Because of the tilt angle, the protection layer casts shadows on the drain and source area [21]. As long as the wafer is rotated in proper position, the shadow can be shifted thoroughly out of the drain and source area in the rectangular devices. The shadow strip forms a part of series resistance attached to the channel and can contribute to 1/f noise. To verify shadow effects on 1/f noise,

we have a big size rectangular device and a 90° oriented rectangular device. So essentially one device will have shadow effect and other device will not have any. Note that shadow effect cannot be avoided in the concentric device of Figure 6.2. In some of the newer processes (such as the one we have used – STI process), shadow effect can be eliminated completely because of the advanced processing steps.

A summary of all the test structures in both the processes appear in the Table A.1 and A.2 in Appendix A. Floorplan and layout of test bar are shown in Table A.3 and Figure A.1 of Appendix A respectively in which location of each structure is indicated. A layout used for different test structures themselves are shown in Figures A.2 to A.9 of Appendix A.

CHAPTER 7

EXPERIMENTAL RESULTS

A major emphasis in this research is on the experimental characterization of the test devices. This experimental characterization is necessary to test the hypothesis stated in Sec 4.2 about whether enhanced current flow in the bird's beaking will degrade (or enhance) the 1/f noise performance. Although ancillary to the original hypothesis, three other issues requiring experimental characterization arose throughout this research initiative. One is the issue of experimental verification of consistency in series connected devices. A second is the issue of the effects of bias and operation region on the 1/f noise performance. A third relates to how the parameters of models which are known to be inaccurate should be extracted to make the models as useful as possible. Finally, the issue of process dependence and in particular the issue of how a reduction in thickness of gate oxide may affect 1/f noise performance was given preliminary consideration. Measuring and extracting the correct data is one of the most challenging and important tasks associated with understanding noise mechanisms. All measurements were performed at the wafer level at room temperature. All test structures were included in both a 2μ BiCMOS process and the 0.18μ STI process. Both processes are commercial processes used by Texas Instruments, Inc. and were briefly discussed in Chapter 6.

In the BiCMOS process, the minimum drawn length and width are 2μ and 2.5μ. The minimum effective width and length are 2μ and 2.5μ. In the STI process, the minimum drawn length and width are 0.6μ and 0.6μ. The effective length and width are 0.18μ (0.35 * L_{drawn} – 0.03) and 0.21μ (W_{drawn} * 0.35) respectively. The PMOS transistors in the BiCMOS

process are not affected by the SDD(Singly Doped Drain) layer. Transistors in all of the test structures were individual devices without any input or output protection circuits. Guard rings were provided for all n- and p-channel structures. Results in the STI process will not be discussed here.

The measurement setup is shown in Figure 5.1 in and the measurement procedure is explained in Section 5.2. Measurements were carried out in the Spice Modeling Lab at Texas Instruments in Dallas, Texas. Guard ring was not biased in NMOS transistor and was biased in PMOS transistor.

7.1 Bird's beaking noise effects

Table 7.1 shows measured data for NMOS and PMOS devices for rectangular, circular, concentric and multiple devices in parallel (55 in this case) test devices for the 2μ BiCMOS process. All four test structures have ideally the same effective W/L of 150/10. The structure with multiple devices in parallel is explained in Section 6.1 case (d) and as explained, has maximum bird's beaking among the four structures.

In these measurements, the Kf parameter extraction algorithm depicted in Figure 5.3 was used. All parameter extractions were based upon fitting to the saturation region model of equation (3) of Chapter 5, i.e.

$$S_i = \frac{K_f I_{ds}}{L_{eff}^2 f^{AF}} \tag{1}$$

Spectral density measurements were taken at 801 data points, a preliminary linear fit to the data was made, the 20 data points deviating the most from this fit were discarded, this process was repeated twice to remove 40 data points total and a final fit was made. The parameter AF was also extracted but is not included in the table.

Table 7.1 – Comparison of rectangular, circular, concentric and 55 devices in parallel (Bird's beaking noise effects)

Data for NMOS – comparison of rectangular, circular, concentric and multiple devices in parallel (W/L =150/10)															
Rectangular (Vgs=1.5, Vds=4)				Circular (Vgs=1.5, Vds=4)				Concentric (Vgs=1.5, Vds=4)				55 devices in parallel (Vgs=1.55, Vds=4)			
Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)	Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)	Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)	Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)
63	186.7	1.218e-13	0.69%	63	189.2	7.426e-14	0.65%	63	189.4	8.668e-14	0.73%	63	185.9	1.194e-13	0.72%
43	188.3	8.395e-14	0.62%	43	191	6.738e-14	0.75%	43	189.7	8.799e-13	0.56%	43	186.3	1.05e-13	0.59%
44	181.2	9.991e-14	0.7%	44	183.5	7.87e-14	0.71%	44	183.66	1.097e-13	0.91%	44	180.14	1.047e-13	0.68%
45	181.66	1.217e-13	0.78%	45	185.3	1.089e-13	0.84%	45	185.72	9.5e-14	0.99%	45	181.08	1.216e-13	0.71%
46	185.3	8.53e-14	0.67%	46	Bad Measurement			46	189.3	8.103e-14	0.71%	46	186.12	1.119e-13	0.69%
33	190	9.958e-14	0.69%	33	192.7	8.03e-14	0.82%	33	193.02	1.081e-13	0.94%	33	189.82	1.234e-13	0.74%
34	189.3	1.184e-13	0.72%	34	191.9	5.769e-14	0.61%	34	191.66	7.880e-14	0.76%	34	187.12	9.758e-14	0.64%
K_f avg = 1.0438e-13				**K_f avg = 7.787e-14**				**K_f avg = 9.322e-14**				**K_f avg = 1.1194e-13**			

Data for PMOS – comparison of rectangular, circular, concentric and multiple devices in parallel (W/L =150/10)															
Rectangular (Vgs=-3.5, Vds=-4)				Circular (Vgs=-3.5, Vds=-4)				Concentric (Vgs=-3.5, Vds=-4)				55 devices in parallel (Vgs=-3.5, Vds=-4)			
Die #	$-I_{ds}$ (μA)	K_f (Am^2)	RMS err (%)	Die #	$-I_{ds}$ (μA)	K_f (Am^2)	RMS err (%)	Die #	$-I_{ds}$ (μA)	K_f (Am^2)	RMS err (%)	Die #	$-I_{ds}$ (μA)	K_f (Am^2)	RMS err (%)
104	739.36	4.911e-15	1.29%	104	734.7	7.968e-15	0.58%	104	728.3	4.869e-15	0.77%	74	756.5	5.639e-15	0.76%
44	762.6	6.126e-15	0.88%	44	759.1	3.691e-15	0.88%	44	752.9	5.429e-15	0.65%	104	735.9	2.344e-14	0.61%
45	761.9	4.501e-15	0.77%	45	759.44	4.310e-15	0.77%	45	751.3	1.799e-14	0.66%	44	760.16	5.161e-15	0.81%
46	756.1	5.05e-15	0.84%	46	748.8	1.196e-14	2.45%	46	745.2	4.490e-15	0.78%	45	751.62	4.805e-15	0.79%
33	748.7	7.381e-15	0.94%	33	747.4	4.26e-15	0.88%	33	742.8	4.162e-15	0.95%	46	749.2	4.683e-15	0.81%
34	755.1	6.469e-15	0.74%	34	750.7	5.079e-15	0.77%	34	744.8	7.197e-15	0.67%	33	741.3	4.504e-15	0.74%
76	774.5	5.91e-15	0.8%	76	759	5.681e-15	0.71%	76	753.9	3.53e-15	0.83%	34	745.2	6.119e-15	0.71%
66	762	3.742e-15	0.9%	66	756.9	5.34e-15	1.11%	66	749.4	4.898e-15	0.84%	76	760.9	7.287e-15	0.68%
K_f avg = 5.511e-15				**K_f avg = 5.19e-15** (Ignoring data on 46)				**K_f avg=4.94e-15** (Ignoring data on 45,76)				**K_f avg=5.457e-15** (Ignoring data on 104)			

Additional (compensation) devices in the multiple devices in parallel structure were connected in the circuit for both NMOS and PMOS case to get the same effective width as rectangular one. From the number of experiments, the width reduction in NMOS was found as high as 0.8μ instead of 0.33μ maximum mentioned in model files.

For NMOS case, V_{gs} value for multiple devices in parallel structure was increased little bit (1.55 instead of 1.5) compared to other structures in order to get the same current level. Bias point was chosen such a way that device plus system noise was clearly distinguishable from system noise alone. Average K_f values for all four cases are shown in table 7.1. RMS error of fitted optimized data is also shown in table. RMS error of less than one percent is usually considered a good data. As seen from data, for NMOS transistors noise for circular and concentric case is lower than that of rectangular case and fifty devices in parallel but difference in K_f magnitude is not very significant. If bird's beaking was a significant issue for 1/f noise, fifty devices in parallel structure would have had lot higher flicker noise than other structures since it has lot of bird's beaking. I would also like to note at this point that device size is 150/10, which is quite large (and that is what analog designers typically use). Hence, area of bird's beaking in normal rectangular structure would be almost negligible but the structure with multiple devices in parallel has lot of bird's beaking. Data for PMOS also supports the same conclusion as NMOS case. As in NMOS case, circular and concentric structures have lower noise than rectangular case but again the difference is not very significant. K_f value in PMOS transistor is an order of magnitude lower than NMOS. While calculating average K_f value, bad measurement data was not included as indicated in table 7.1 for PMOS. Bad measurement could be due to typical environment while making that particular measurement or it could be a typical bad device. Since PMOS devices have

inherently lower noise than NMOS, V_{gs} was increased compared to NMOS in order to get higher current and hence higher noise. Only then it was possible to separate PMOS device plus system noise compared to system noise alone due to resolution of the system. For PMOS, V_{gs} value was not needed to increase in the case of multiple devices in parallel structure compared to other structures and hence width reduction (ΔW) should be less here compared to NMOS case. We were not able to compare 1/f noise for structures in Figure 6.1 alone independently because of much more bird's beaking than expected.

7.2 Flicker noise in series connected devices

We have different structures to verify noise in series connected transistors. As explained in section 2.2.2, if there are more than two transistors connected in series with the effective W/L same as a single equivalent transistor, the top device will be in saturation and rest all in linear region. But since the effective W/L ratio in both cases is same and if the total dc current is also held constant, flicker noise should be same. To verify this effect, we have here four different structures: single device with W/L of 40/40, two 40/20 devices in series, ten 40/4 devices in series and twenty 40/2 devices in series. All of them have same effective W/L of 40/40.

Figure 7.1 in the next page shows comparison of drain current noise density for four different structures discussed above for NMOS. As seen in figure, flicker noise progressively increases as we increase the number of devices in series. Although there is not much increase in noise from ten to twenty devices in series (they are even overlapping sometimes), increase is clearly visible from one-two devices to ten-twenty devices. Figure 7.2, shows two extreme cases i.e., one device alone and twenty devices in series. As we will see from other results

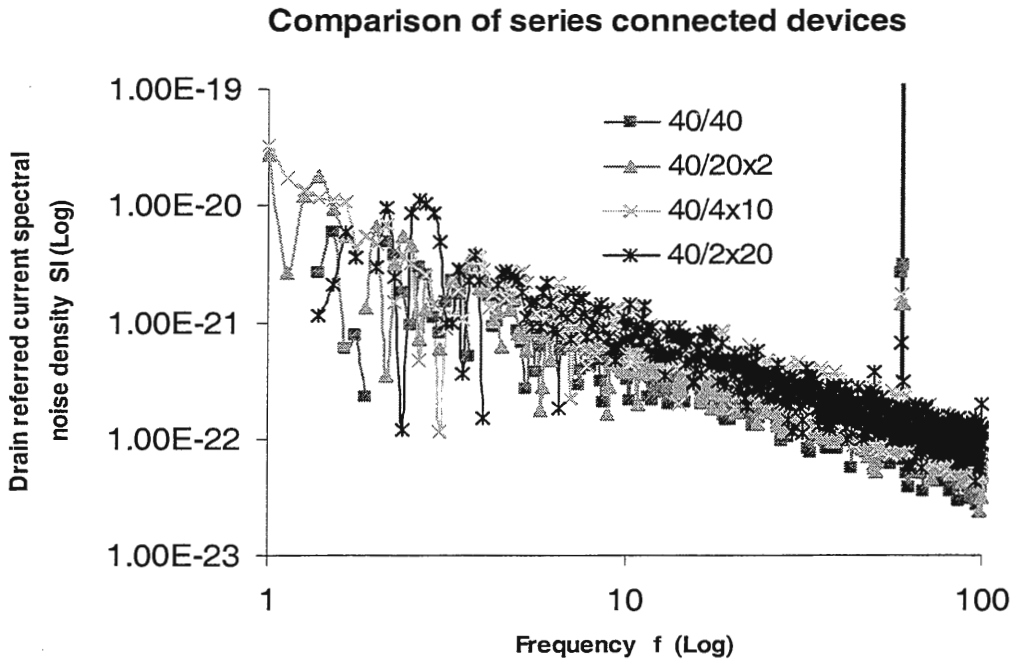


Figure 7.1 - Flicker noise in series connected device

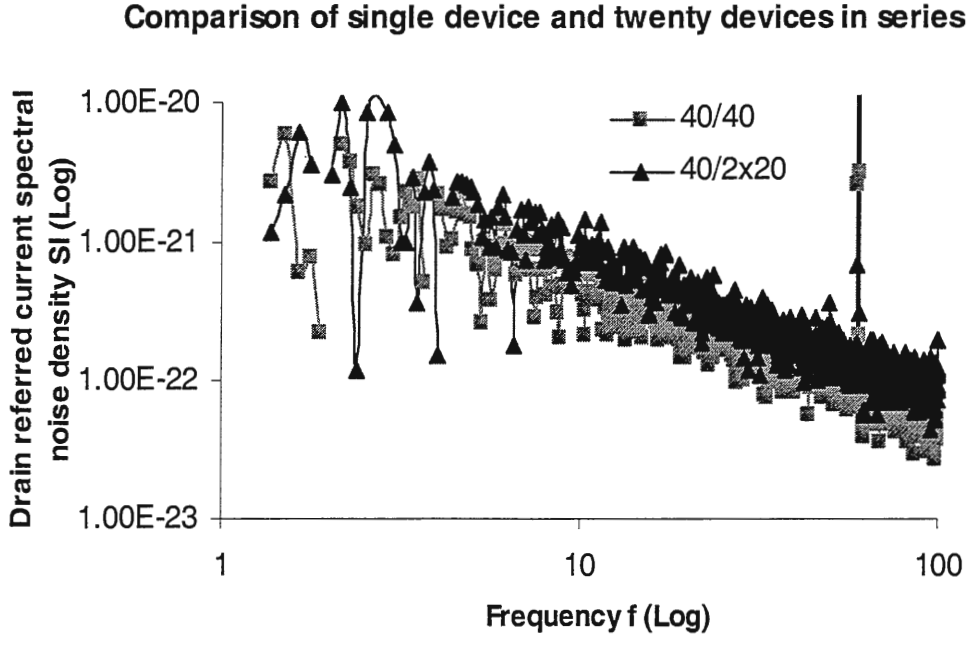


Figure 7.2 - Comparison of 1/f noise between single device and twenty devices in series

that for the same Vgs, flicker noise in the linear region should be lower than saturation region since current is lower in linear region. But instead, we find higher noise in twenty devices series configuration. The reason for that could be poly resistance for one big device versus twenty devices in finger structure and additional contact resistance for multiple devices in series configuration.

Flicker noise co-efficient (K_f) values for a particular bias point (V_{gs} = 3, V_{ds} = 5) for eight different die locations on a wafer are shown in table 7.2. Bias point is selected in deep saturation. As seen from K_f values, flicker noise progressively increases from one device to twenty devices in series although, there is not much difference in K_f as we increase the number of devices from ten to twenty. In fact, some of the numbers are overlapping as seen from column three and four of table 7.2. Figure 7.3 shows K_f comparison graphically for four different configurations as discussed where configuration one to four corresponds to 40/40, 40/20x2 (2 in series), 40/4x10 (ten in series) and 40/2x20 (twenty in series) respectively. Connection among the points is just for the aid of eye. Average K_f values are plotted in bold line.

Because of high length (40μ) of these structures, overall noise is lower and it is quite comparable to system noise in low frequency region of f=1 to f=10 Hz. However, extracting the K_f and device noise from f=10 to f=100 Hz alone gives the same conclusions as well.

7.3 Operating region and bias dependence of flicker noise

There are controversies of bias dependence of flicker noise. Bias dependence is also associated with technology and operation region. It is more prevalent at certain bias points than others.

Table 7.2 – Comparison of rectangular series connected devices

Data for NMOS – comparison of rectangular series connected devices (Vgs=3, Vds=5 for all devices)															
Single device 40/40				Two 40/20 device in series (40/20x2)				Ten 40/4 devices in series (40/4x10) (trimming is used to compensate ΔL)				Twenty 40/2 devices in series (40/2x20) (trimming is used to compensate ΔL)			
Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)	Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)	Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)	Die #	I_{ds} (μA)	K_f (Am^2)	RMS err (%)
73	100.04	9.247e-14	0.71%	73	100.4	8.074e-14	0.71%	73	104.74	1.536e-13	0.64%	73	100.54	1.666e-13	0.72%
64	96.83	1.006e-13	0.79%	64	97.12	1.324e-13	0.82%	64	96.72	1.398e-13	0.56%	64	97.42	1.881e-13	0.49%
55	97.54	8.87e-14	0.65%	55	97.92	1.003e-13	0.59%	55	98	6.815e-11 (Bad Data)	0.66%	55	98.14	1.858e-13	0.56%
53	99.61	1.008e-13	0.67%	53	99.73	1.313e-13	0.74%	53	99.97	1.36e-13	0.7%	53	96.44	2.536e-12 (Bad Data)	0.59%
74	96.99	9.284e-14	0.74%	74	97.2	1.303e-13	0.82%	74	96.71	1.932e-13	0.57%	74	97.77	1.732e-13 (Bad Trim)	0.68%
44	97.73	8.273e-14	0.63%	44	98.1	9.847e-14	0.76%	44	95.1	1.325e-13	0.51%x	44	94.42	1.365e-13	0.71%
45	98.19	8.852e-14	0.82%	45		Bad Data		45	97.99	3.487e-13	0.62%	45	94.86	1.834e-13	0.71%
46	99.24	1.104e-13	0.71%	46	99.61	1.028e-13	0.94%	46	99.2	1.406e-13	0.65%	46	99.86	1.566e13	0.71%
K_f avg = 9.47e-14				**K_f avg = 1.109e-13** (Discarding data on 45)				**K_f avg = 1.752e-13** (Discarding data on 55)				**K_f avg = 1.7e-13** (Discarding data on 53,74)			

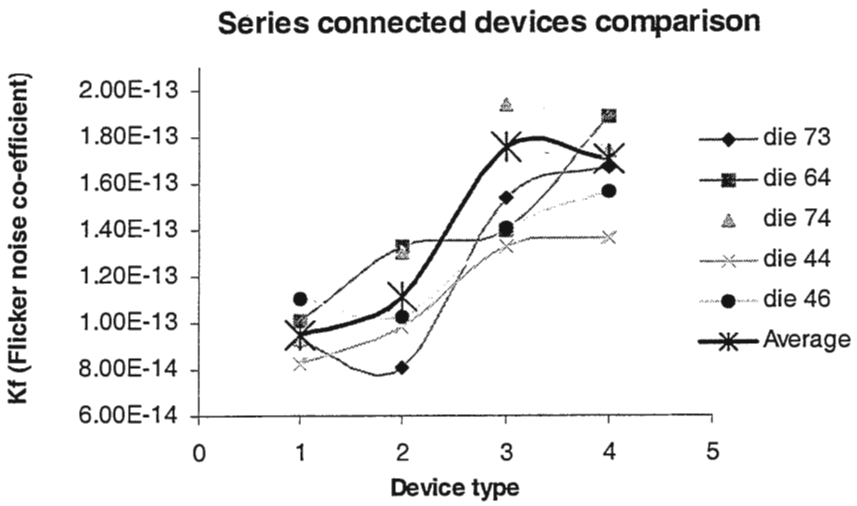


Figure 7.3 - K_f comparison for series connected devices

To understand bias dependence of flicker noise, we chose one particular test device with W/L of 32/4. The corresponding measurement parameters and flicker noise co-efficients are summarized in table 7.3. With two different levels of high and low Vgs, Vds was varied to get different bias points in linear region. Nominal v_t of the device was 0.7V. As mentioned in Table 7.3, K_f can vary as much as 8x-10x. Drain referred current noise spectral density for this device for different bias conditions of Vgs=2V and Vds=0.2,0.4,0.8,1.2V is shown in Figure 7.4. As expected, increasing the drain voltage in linear region increases the device current and since flicker noise is directly proportional to dc current of the device, noise increases. In fact, during these set of measurements we noticed that flicker noise co-efficient was lower for Vgs = 3.5 case compared to Vgs = 2 case as shown in Figure 7.5. This led us to our next set of measurements for verifying Vgs dependence alone.

Table 7.4 summarizes the measurement details for Vgs variation for 3 different dies. Figure 7.6 shows the K_f variation graphically. As shown in Figure 7.6, variation in V_{gs} could be as much as an order (10x) in magnitude.

Table 7.3 – V_{ds} dependence of flicker noise for NMOS 32/4

Bias dependence for NMOS transistor with W/L = 32/4												
Die #	Vgs = 2, Vds = 0.2			Vgs = 2, Vds = 0.4			Vgs = 2, Vds = 0.8			Vgs = 2, Vds = 1.2		
	I_{ds} (uA)	K_f (Am^2)	RMS err (%)	I_{ds} (uA)	K_f (Am^2)	RMS err (%)	I_{ds} (uA)	K_f (Am^2)	RMS err (%)	I_{ds} (uA)	K_f (Am^2)	RMS err (%)
66	82.54	8.108e-15	0.57%	146.02	2.182e-14	0.54%	223.1	6.595e-14	0.51%	246.6	1.067e-13	0.49%
65	81.56	1.237e-14	0.57%	145.12	2.828e-14	0.53%	220.9	5.939e-14	0.58%		Bad data	
55	82.5	1.322e-14	0.56%	146.96	3.118e-14	0.58%	224.4	8.119e-14	0.57%	245.16	1.192e-13	
95	81.25	1.241e-14	0.56%	144.58	3.261e-14	0.55%	220.1	8.134e-14	0.60%	242.92	9.52e-14	0.54%
74	83.14	1.643e-14	0.58%	148.1	3.726e-14	0.53%	226.4	6.782e-14	0.54%	250.5	9.353e-14	0.51%
84	81.05	1.382e-14	0.63%	144.2	3.022e-14	0.59%	219.5	6.473e-14	0.53%	242.2	7.956e-14	0.54%
	Kf avg = 1.273E-14			**Kf avg = 3.023E-14**			**Kf avg = 7.007E-14**			**Kf avg = 9.88E-14**		

Die #	Vgs = 3.5, Vds = 0.2			Vgs = 3.5, Vds = 0.4			Vgs = 3.5, Vds = 0.8			Vgs = 3.5, Vds = 1.2		
	I_{ds} (uA)	K_f (Am^2)	RMS err (%)	I_{ds} (uA)	K_f (Am^2)	RMS err (%)	I_{ds} (uA)	K_f (Am^2)	RMS err (%)	I_{ds} (uA)	K_f (Am^2)	RMS err (%)
66	173.54	3.31e-15	0.83%	331.5	1.009e-14	0.55%	600.76	2.302e-14	0.54%	806.42	2.958e-14	0.54%
55	173.06	4.921e-15	0.77%	330.56	1.236e-14	0.55%	599.2	2.742e-14	0.64%	804.5	3.836e-14	0.68%
95	171.56	3.618e-15	0.81%	327.64	1.046e-14	0.56%	593.5	2.299e-14	0.58%	796.34	3.365e-14	0.59%
74	174.8	5.535e-15	0.83%	333.7	1.541e-14	0.67%	604.9	2.898e-14	0.57%	812.1	5.189e-14	0.55%
84	172.3	4.93e-15	0.88%	328.9	1.361e-14	0.60%	595.7	2.524e-14	0.55%	799.2	4.018e-14	0.54%
	Kf avg = 4.463E-15			**Kf avg = 1.239e-14**			**Kf avg = 2.553e-14**			**Kf avg = 3.879e-14**		

Table 7.4 – V_{gs} dependence of flicker noise for NMOS 32/4

Bias condition		Die 66			Die 55			Die 95			
Vgs (V)	Vds (V)	Idc (uA)	K_f (Am^2)	RMS err (%)	Idc (uA)	K_f (Am^2)	RMS err (%)	Idc (uA)	K_f (Am^2)	RMS err (%)	**Kf avg**
1.8	0.8	168.8	1.104e-13	0.53%	169.1	9.675e-14	0.58%	164.9	1.029e-13	0.68%	**1.034e-13**
2	0.8	223.06	6.595e-14	0.51%	224.42	8.119e-14	0.57%	220.1	8.134e-14	0.60%	**7.616e-14**
2.4	0.8	332.9	3.544e-14	0.54%	333.6	5.190e-14	0.61%	327.7	4.378e-14	0.62%	**4.371e-14**
2.8	0.8	435	2.640e-14	0.53%	436	4.135e-14	0.66%	429.3	3.047e-14	0.63%	**3.274e-14**
3.2	0.8	531.7	2.174e-14	0.53%	532.9	2.728e-14	0.57%	525.2	2.329e-14	0.63%	**2.410e-14**
3.5	0.8	600.76	2.302e-14	0.54%	599.18	2.742e-14	0.64%	593.5	2.299e-14	0.58%	**2.448e-14**

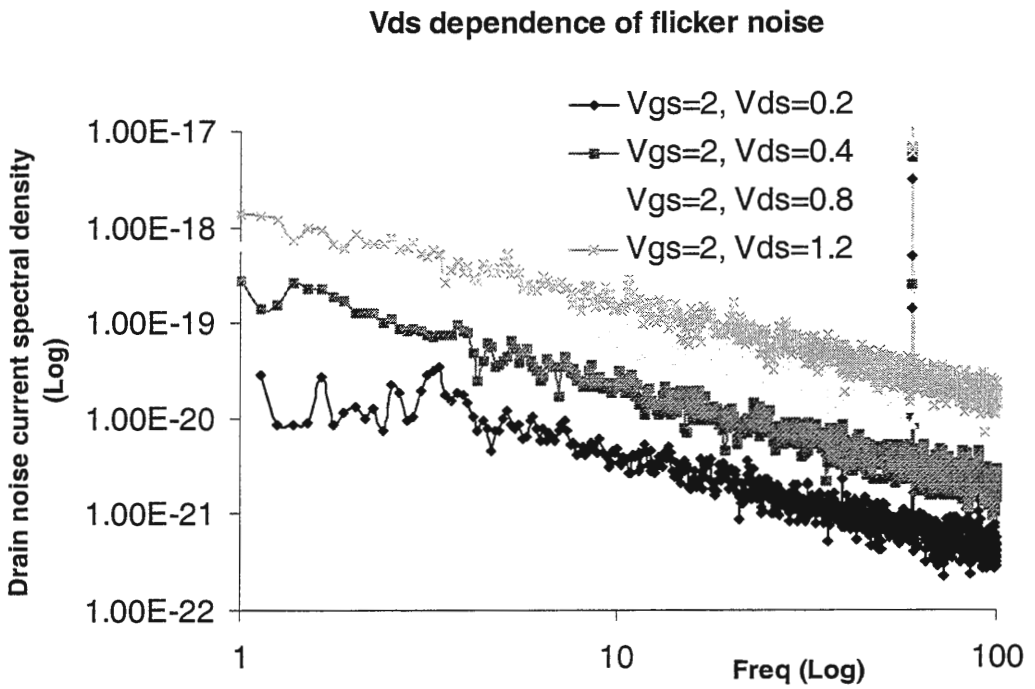


Figure 7.4 - Bias dependent flicker noise

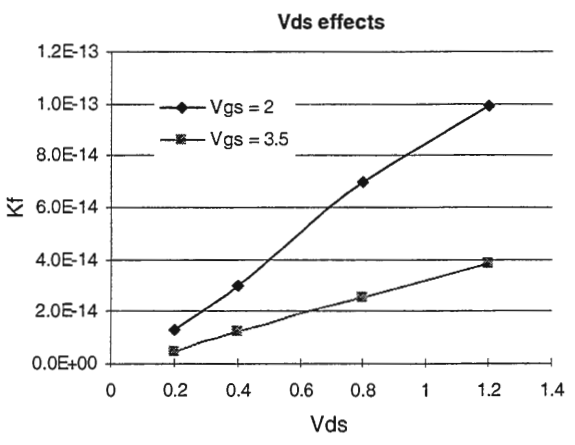


Figure 7.5 - Vds dependence of flicker

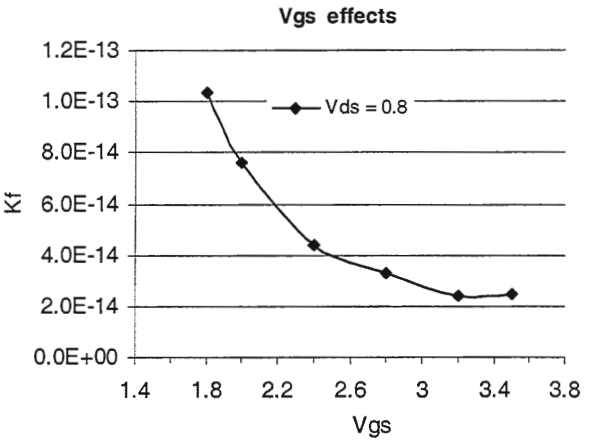


Figure 7.6 - Vgs dependence of flicker

7.4 New algorithm for data extraction

7.4.1 Need for new algorithm

Flicker noise coefficient (K_f) measurement procedure is described in detail in section 5.3. As mentioned in equation (9) of Chapter 2, current exponent is assumed to be 1. The noise analyzer used for 1/f noise measurements is HP35670. It performs linear sweep for the frequency span of f=1Hz to f=100Hz and hence we have 80 data points in first frequency decade and 720 data points in second frequency decade. As given by equation (2) of Chapter 5, corrected flicker noise for a MOS device is given by,

$$S_N = \frac{(S_{NO} - S_{BO})(1 + g_{ds}R_L)^2}{A_v^2 \bullet R_L^2} \qquad (2)$$

where S_N is the noise current spectral density of the DUT, S_{NO} is the spectral density at the output of the noise amplifier, S_{BO} is the spectral density at the output of the noise amplifier without the DUT in the circuit, g_{ds} is the small signal output impedance of the DUT, A_V is the voltage gain of the amplifier. We then plot this linear sweep data on log scale to extract K_f.

(1) The current algorithm used by internal software of Texas Instruments gives equal weight to all frequency points and because there are only 80 data points in first decade compared to 720 data points in second decade, it gives almost all weightage to second decade.

(2) We always have spike at 60 Hz and sometimes depending on environment condition we also get spike at some other frequencies. With TI algorithm, location of spike could affect the final extracted value of Kf and by default only 60 Hz spike is taken cared of by internal software. In other words, you have to remove manually other data

spikes in order to get cleaner extraction. So, flicker noise co-efficient extraction values, to a certain extent, depends on the person handling the system. In other words, operator becomes the GOD.

We didn't want this to happen. We have designed here an algorithm to extract Kf values from the noise data. It uses weighted linear regression analysis. It has a weight vector W = 1/f. In other words, higher frequencies have lower weight which makes sense since flicker noise also decreases as frequency increases. The lower frequency components (lower decade) are more representative of the 1/f noise than upper decade. (Well ideally, they should have same slope since energy per decade of bandwidth should be ideally same.) In our algorithm, we also take care of the spikes occurring intermittently in measurement. We have two phase in the algorithm:

1) Phase 1 - In this phase we remove 20 data points (out of 800) which have highest deviation from fitted line. Fitted line is constructed with weighted linear regression analysis. We throw away those 20 data points from total data points. A line y = a + bx is fitted to this corrected data of equation (1) of Chapter 5 with the following equation,

$$Error = \sum_{i=1}^{n} w_i \left(\overline{y} - (a + bx)\right)^2 \qquad (3)$$

where weight w_i is assumed to be 1/f. Intercept of this fitted line to the y-axis gives corrected flicker noise spectrum density S_N of (2). Since the algorithm automatically removes 20 data points, operator will not come into picture.

2) Phase 2 - In this phase, we fit the data obtained in phase 1 and then reapply the weighted regression analysis to throw away next set of 20 worst data points and thus totally remove 40 data points with maximum deviation from fitted line.

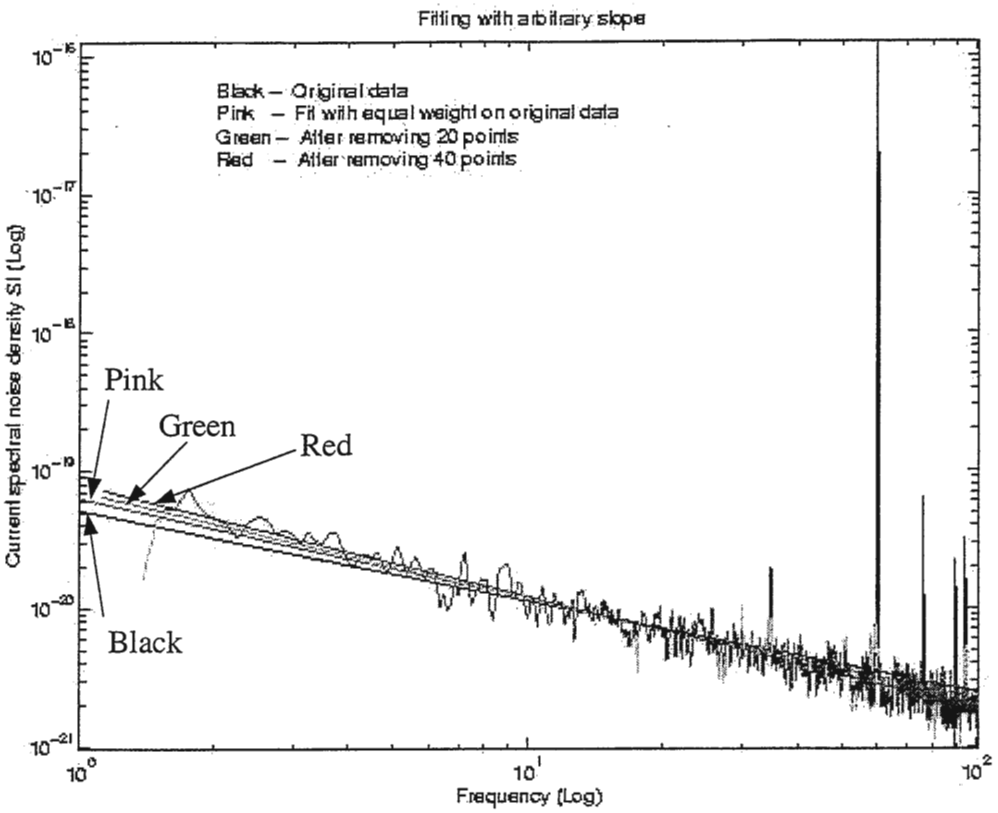


Figure 7.7 - K_f extraction with new algorithm

Accurate flicker noise coefficient is extracted from these 760 data points with weighted regression analysis and used in calculation. Slope of the final fitted line gives the current exponent AF in equation (1) of Chapter 5 and is not equal to one.

Figure 7.7 shows this graphically. Black line is original data collected by Dynamic Signal Analyzer (DSA) which contains some arbitrary spikes due to environment conditions. Pink line shows the fitted line with equal weight on all the data points and with arbitrary slope i.e. slope could be other than –1. Green and red line show the fitted lines after applying weighted regression analysis two times on the extracted data. Notice that intercept of line, which is directly proportional to K_f , varies significantly after regression analysis. This is a much better approximation of K_f than the other case. Slope of this final fitted line gives the flicker noise current exponent AF which happens to be –0.8167 for the example of Figure

7.7. RMS error is also found to be lesser with new algorithm, which leads to more confidence in data extraction.

CHAPTER 8

CONCLUSIONS, CONTRIBUTIONS AND FUTURE WORK

Because low frequency noise is an inseparable parameter in current CMOS/BiCMOS technology, understanding the physical origin of noise to lessen noise and taking advantage of available design variables is highly desirable.

Test structures were fabricated in two different processes at Texas Instruments, Dallas. One process was n-well BiCmos process that has SDD (Singly Doped Drain) devices. This process has a nominal oxide thickness of 425 A°, nominal V_T of 0.7V, and a maximum supply voltage Vdd of 5V. Minimum effective channel length for the devices is 2u and minimum width is 2.5u. PMOS transistors were not affected by the SDD layer. The second process was a more advanced Shallow Trench Isolation (STI) n-well CMOS process[28]. In the STI process, a "trench" filled with oxide isolates devices from one another thereby allowing the devices to be packed closer to each other without compromising latchup immunity. This STI process has a gate oxide thickness of 40 A°, a maximum Vdd of 1.8V and it also has an analog friendly low V_T device in addition to a higher V_T device. The minimum drawn channel length is 0.49um and the minimum effective channel length is 0.45um. Results in the STI process will not be discussed in detail in this thesis because the processing was not completed until after the bulk of this thesis was completed.

Transistors in the test structures were individual devices without any input or output protection circuits. Guard rings were provided for all n- and p-channel structures. As the title of the thesis suggests, main focus of this work was to characterize 1/f noise in bird's beaking region of MOS transistor. However, due to gross inconsistencies found in both measurements

and simulations, major part of this work was refocused on noise modeling and noise measurements and hence we were able to make a significant contributions in these areas as well. The summary of our conclusions follows:

(1) The concept of consistency in noise models for active devices was introduced. From this formulation, fundamental properties of the spectral density of a consistent model were developed.

(2) It was shown that the noise in a transistor whether operating in the saturation or triode region is essentially determined by the noise in a triode region device. This suggests that noise modeling research for MOS devices should be focused on the triode region of operation.

(3) It was shown that some of the most widely used thermal and 1/f noise models for MOS transistors are inconsistent and thus inherently incorrect. These inconsistencies can introduce substantial errors when these models are used to predict the effect of noise in practical circuits. We have shown in chapter 4 that by having separate K_f for triode region of operation and the saturation region of operation, a more accurate prediction of the total device noise is obtained.

(4) Bird's beaking doesn't play a significant role in 1/f noise for this particular LOCOS process for both NMOS and PMOS. Although results are not shown here, we noticed in our experiments that bird's beaking doesn't play any role in 1/f noise even for the advanced STI process we used in our experiments.

(5) Device geometry (circular or concentric) does help to reduce 1/f noise but the reduction in noise magnitude is marginal (~10%). Experiments were conducted on big devices since analog designers typically use large sized devices. However, for

minimum sized circular and concentric structures we have not verified the results. Because good models for non-rectangular structures are not very well defined, inclusion of those structures in design may not be justifiable.

(6) Increasing the number of devices in series progressively increases 1/f noise. However, after a certain number of devices are connected in series, the increase may not be very significant. The increase in 1/f noise could be attributed to poly resistance for one big device versus multiple transistors in finger structure and additional contact resistance for those transistors, however, we don't have an exact explanation to these experimental observations and future work is required to model these effects.

(7) Flicker noise is bias and operating region dependent. For a given V_{gs}, the saturation region has higher 1/f noise than the linear region due to the higher conduction of current in the device. Lower V_{ds} will give lower current and hence lower noise in the linear region of operaiton. Noise measurements should be always carried out in both the linear and saturation regions. In fact, as we have shown in Chapter 7, the difference in noise spectral density magnitude between the linear and saturation regions could be as high as two order of magnitude which corresponds to 6.5 bit accuracy differences. This could be a significant factor in the design of 10 bits and higher systems.

(8) With the large number of measurements taken, we have observed that variation in K_f is possible from device to device, die to die and lot to lot for a given process. Stochastic characterization of K_f is needed to accurately characterize 1/f noise in a process.

(9) 1/f noise is V_{gs} dependent. The widely used SPICE level 0 model shown in equation (3) of Chapter 3 doesn't show a V_{gs} dependence. As shown in this equation, flicker noise is directly proportional to dc current. For a given V_{ds}, increasing the V_{gs}, increases the dc current and hence one would expect 1/f noise to increase but total 1/f noise decreases with increasing V_{gs} in our experiments. Thus increasing the V_{gs} could be a viable method in some cases to reduce the noise but it may not be feasible all the time.

(10) A new algorithm based on weighted regression analysis was developed for accurate extraction of the flicker noise coefficient from raw data. Not only does the new algorithm fit data better than what is achieved with the current method, but it also removes operator dependency on the result and gives more repeatable and reliable values. We also showed that weighted regression analysis along with arbitrary line fitting (with slope not equal to one) gives the least amount of rms error.

Apart from main conclusions noted above, we would like to note some side conclusions

(11) P-channel devices have generally lower noise compared to n-channel devices for a given process because the channel is farther away from the S_i-S_iO_2 surface compared to n-channel device.

(12) K_f is a process dependent parameter and it could be misleading in some cases. For comparative analytical studies, noise density should be given a preference over K_f.

(13) Accurate 1/f noise measurement is a key issue and guidelines given in chapter 5 should be useful for establishing 1/f noise measurement procedure.

It will be interesting to carry out noise measurements in the subthreshold region. Rigorous accurate measurements are required to further analyze bias dependence, operating

region dependence, area (WL) dependence, width/length effects, series connection of transistors etc. Minimum sized non-rectangular structures would be also interesting.

The inhomogeneous behavior of the channel in saturation makes 1/f noise modeling quite complicated and results in non-user friendly analytical solutions, whether they are based on ΔN or on $\Delta\mu$ considerations [5]. There exists a fundamental misunderstanding of even basic 1/f noise models among the design community. A unified noise model, either empirical or physical, that can predict the noise power in all bias regions has not yet emerged among the analytical model development community. Incorporation of existing models in circuit simulators is far from complete [5] and lot of work is required in that direction.

APPENDIX A

TEST STRUCTURES

A.1 Test structures in LinearBiCmos 2u process

TABLE A.1 – Test structures for 1/f noise characterization in LOCOS process

Module Name	Drawn Device Size	Comments
NBR1	150/10	Rectangular big device, no bird's beaking
NBR2	75/10, two in parallel	Different structures with same effective W/L of 150/10 but with different percentage of bird's beaking. Additional structures to compensate for ΔW are provided for laser trimming to match current accuracy of 1-2 %
NBR3	15/10, ten in parallel (8/10, 4/10,2.5/10 – additional for laser trim)	
NBR4	3/10, fifty in parallel (32/10,16/10, 8/10, 4/10, 2.5/10 – additional for laser trim)	
NBR5	150/10	90° oriented to verify shadow effects
NBR6	32/32,32/16,32/8,32/4,32/2	Structures to verify length effects
NBR7	32/4,16/4,8/4,4/4	Structures to verify width effects
NBR8	40/40, 40/20x2, 40/4x10 (40/5, 40/3, 40/2 additional),40/2x20 (40/8, 40/4, 40/2 additional)	Structures to verify series connection of devices (1, 2, 10, 20 devices in series). Additional structures provided to compensate for ΔL
NBR9	R_{in} = 19.1μ, R_{out} = 29μ	Circular structure with effective W/L of 150/10, same area as rectangular one
NBR10	a = 15.08μ, b = 9.46μ (Figure 6.2)	Concentric structure with effective W/L of 150/10, same area as rectangular one

A.2 Test structures in STI 0.18u process

TABLE A.2 – Test structures for 1/f noise characterization in STI process

Module Name	Drawn Device Size	Comments
STRUCT1_NCH	300/20	Rectangular big device, no bird's beaking
STRUCT2_NCH	150/10, two in parallel	Different structures with same effective W/L of 150/10 but with different percentage of bird's beaking. Additional structures to compensate for ΔW are provided for laser trimming to match current accuracy of 1-2 %
STRUCT3_NCH	75/10, ten in parallel (3/20, 3/20 – additional for laser trim)	
STRUCT4_NCH	6/20, fifty in parallel (12/20,9/20, 6/20, 3/20 – additional for laser trim)	
STRUCT5_NCH	300/20	90° oriented to verify shadow effects
STRUCT6_NCH	60/60,60/30,60/15,60/9,60/3	Structures to verify length effects
STRUCT7_NCH	60/20,30/20,12/20,3/20	Structures to verify width effects
STRUCT8_NCH	60/60, 60/30x2, 60/6x10 (60/9, 60/6, 60/3 additional),60/3x20 (60/6, 60/3, 60/2 additional)	Structures to verify series connection of devices (1, 2, 10, 20 devices in series). Additional structures provided to compensate for ΔL
STRUCT9A_NCH	R_{in} = 38.2μ, R_{out} = 58μ	Circular with effective W/L of 300/20, same area as rectangular – contacts on top of poly (punchthrough possibility)
STRUCT9B_NCH	R_{in} = 38.2μ, R_{out} = 58μ	Circular structure with effective W/L of 300/20, same area as rectangular one – contacts outside poly
STURCT10A_NCH	a = 30.13μ, b = 18.94μ (Figure 6.2)	Concentric structure with effective W/L of 300/20, same area as rectangular one

Note : $L_{eff} = L_{drawn} * 0.35 - 0.03$, $W_{eff} = W_{drawn} * 0.35$

A.3 Layout of test structures

Table A.3 - Floorplan for lbc3s test structures for 1/f noise measurements

NMOS NBR3					1 NMOS NBR2				2 NMOS NBR1		3 NMOS NBR5	
NMOS NBR6					3.1 NMOS NBR7				3.2 NMOS NBR8			
32/32	32/16	32/8	32/4	32/2	32/4	16/4	8/4	4/4	40/40	40/20x2	40/4x10	40/2x20
NMOS NBR4				3.3 NMOS NBR9	3.4 NMOS NBR10		3.5 PMOS NBR1				PMOS NBR9	PMOS NBR10
PMOS NBR6					3.6 PMOS NBR7				3.7 PMOS NBR8			
32/32	32/16	32/8	32/4	32/2	32/4	16/4	8/4	4/4	40/40	40/20x2	40/4x10	40/2x20
4 PMOS NBR3					5 PMOS NBR2				6 PMOS NBR1		7 PMOS NBR5	

This diagram roughly shows the floorplan of LBC3S structures. There are 5 different rows of test structures as shown. Although, locations of the transistors may not be exactly same as shown, they show approximate locations.

xactly same as shown, they show approximate locations.

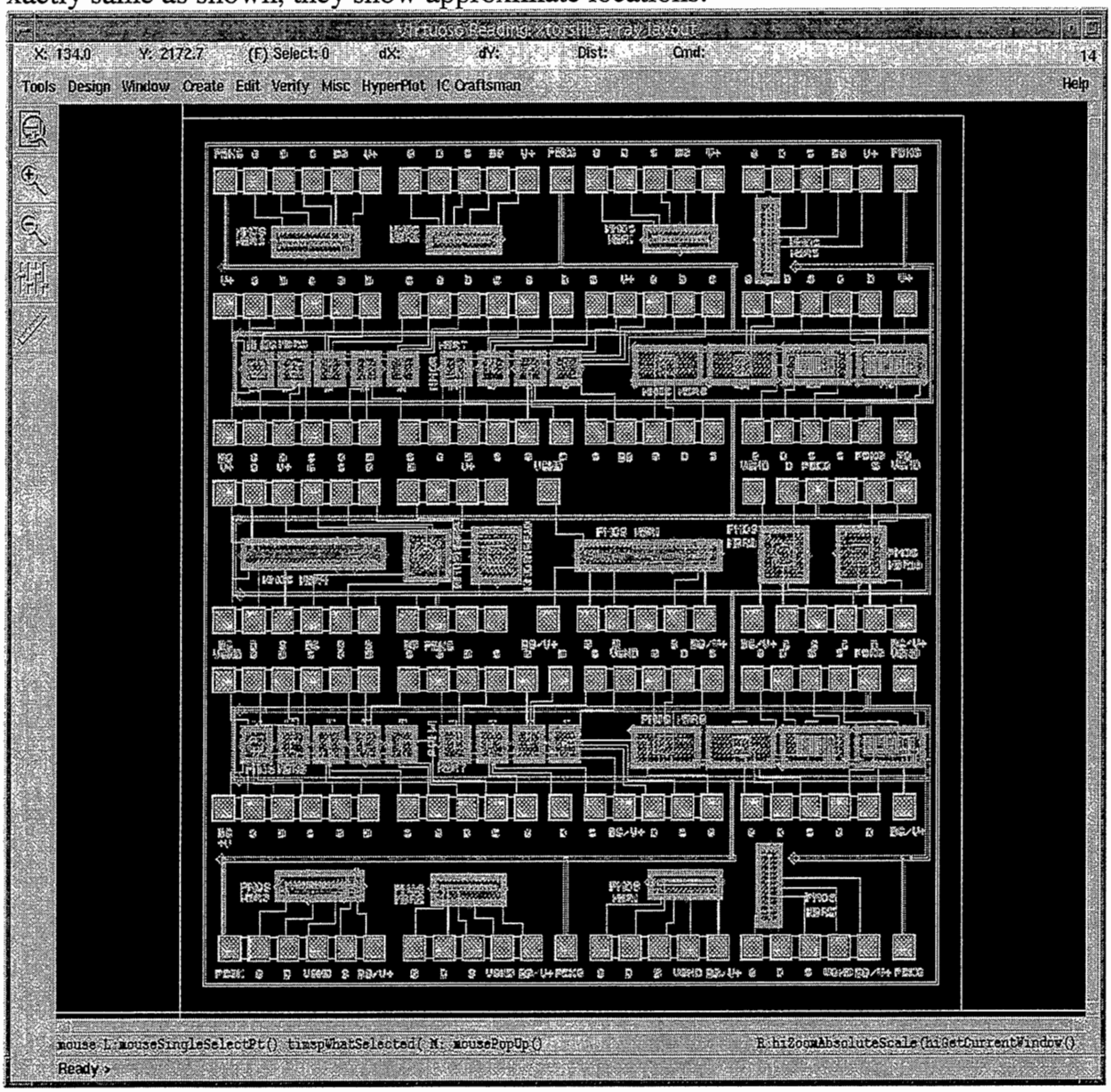


Figure A.1 – Layout of test bar for Linear BiCMOS process

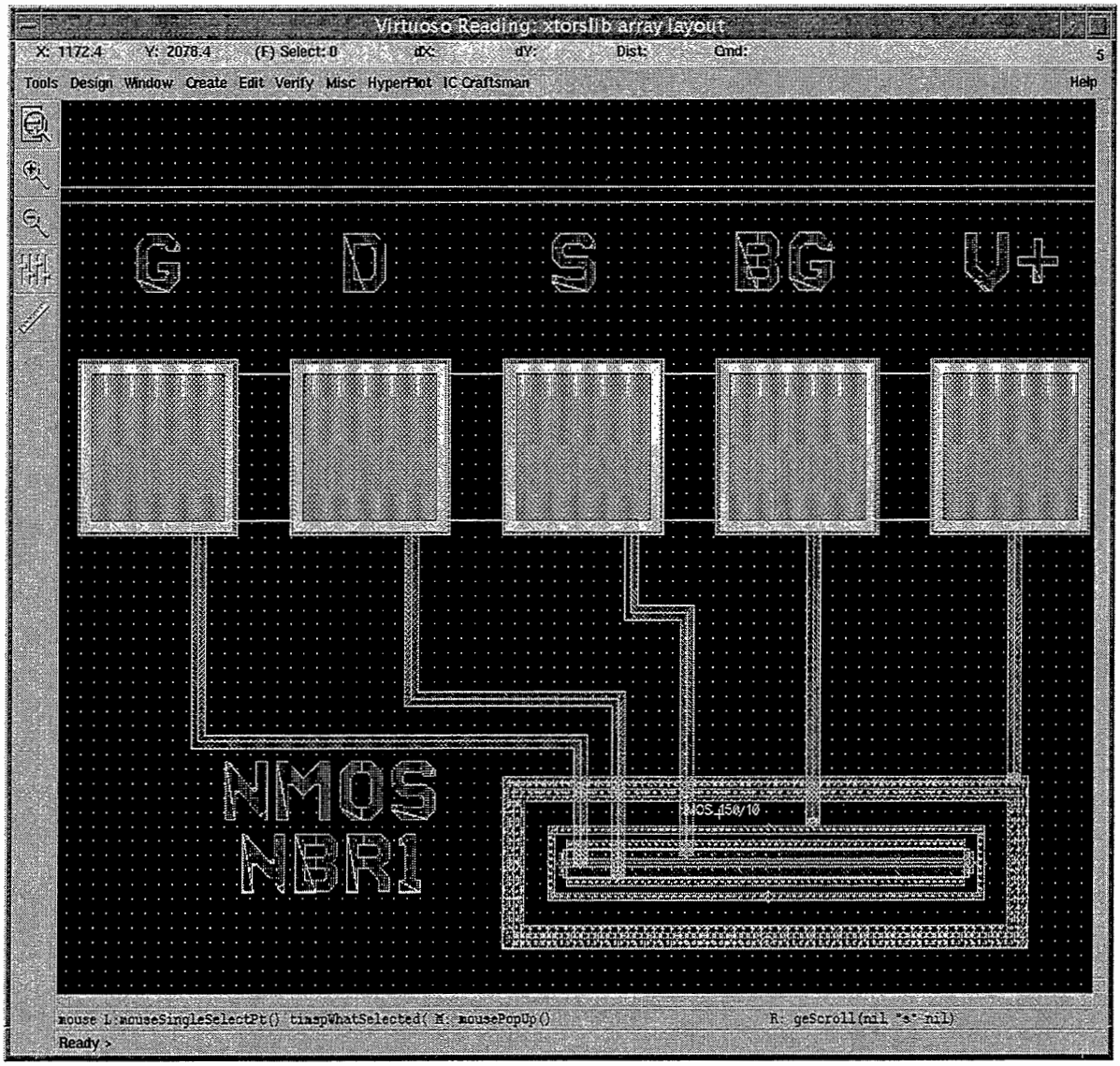


Figure A.2 – Layout of test structure NMOS NBR1 of Table A.1

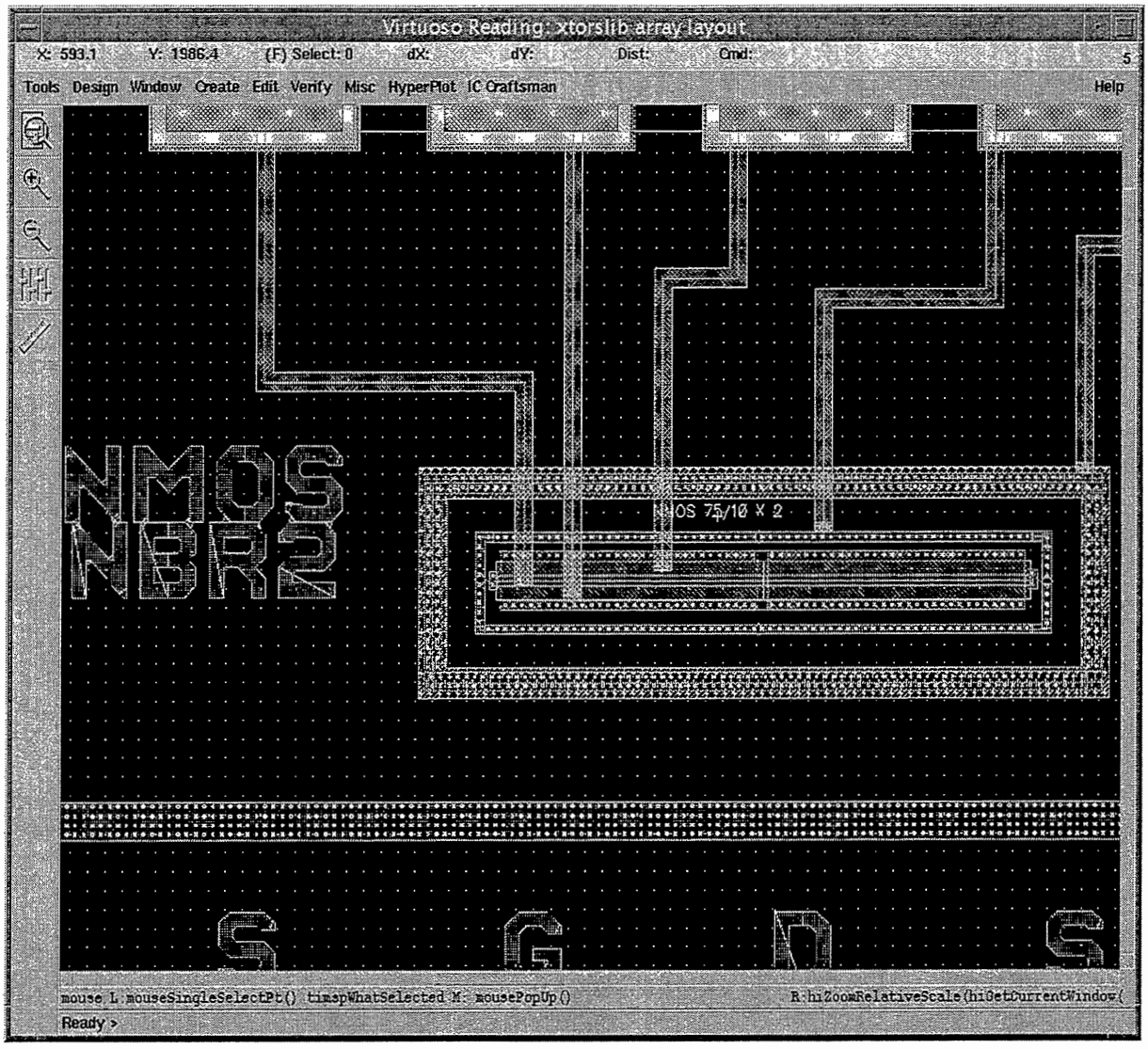


Figure A.3 – Layout of test structure NMOS NBR2 of Table A.1

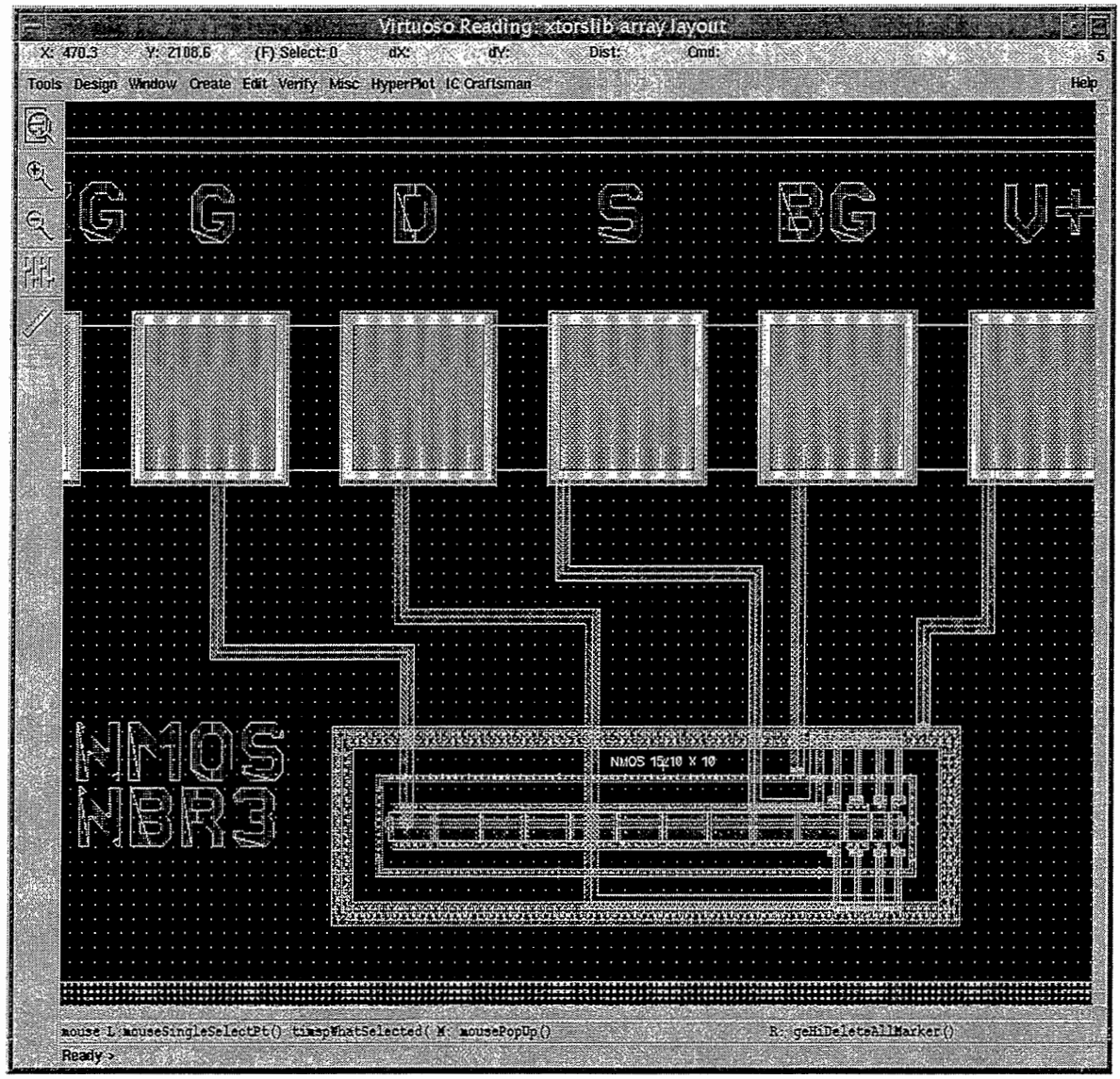


Figure A.4 – Layout of test structure NMOS NBR3 of Table A.1

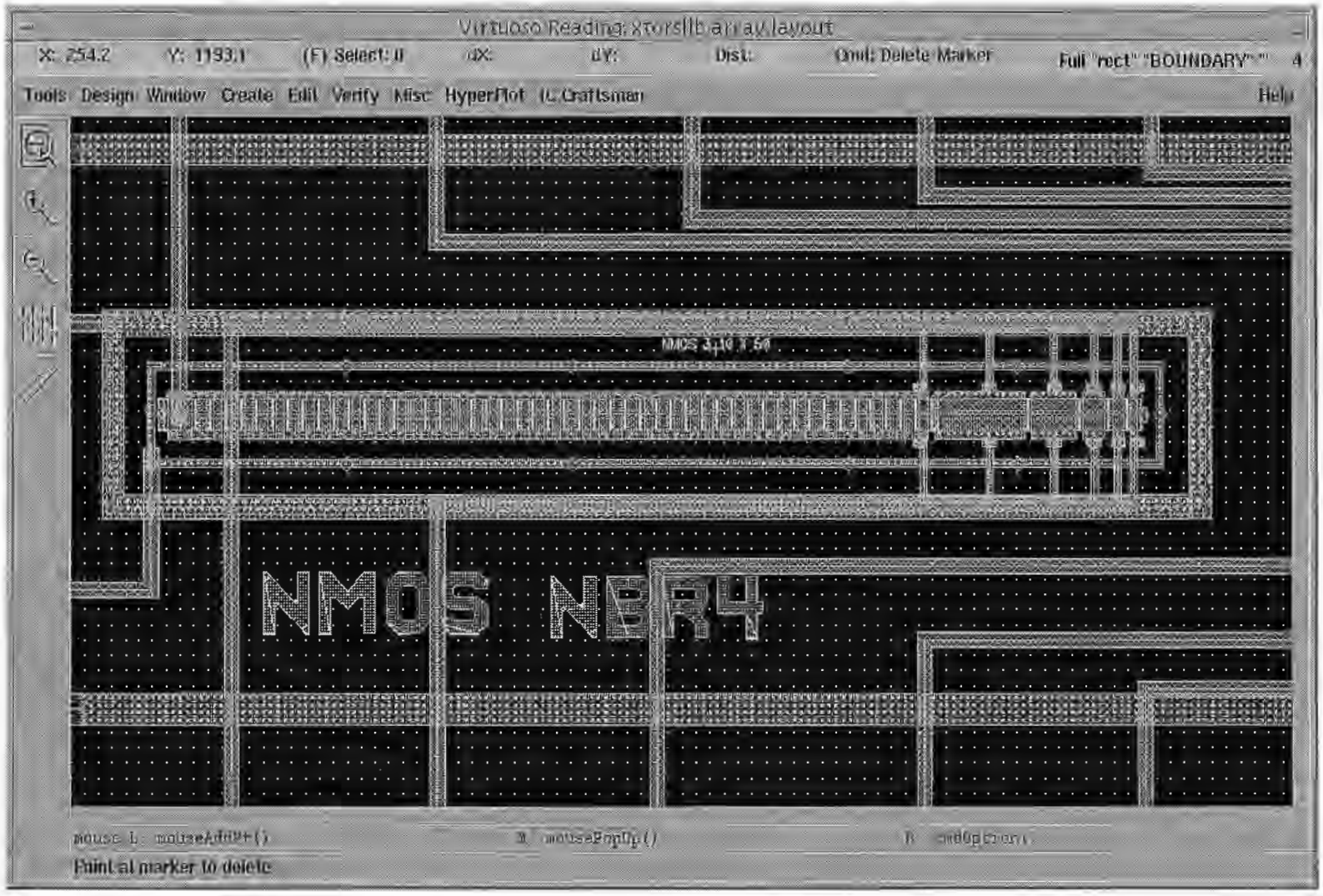


Figure A.5 – Layout of test structure NMOS NBR4 of Table A.1

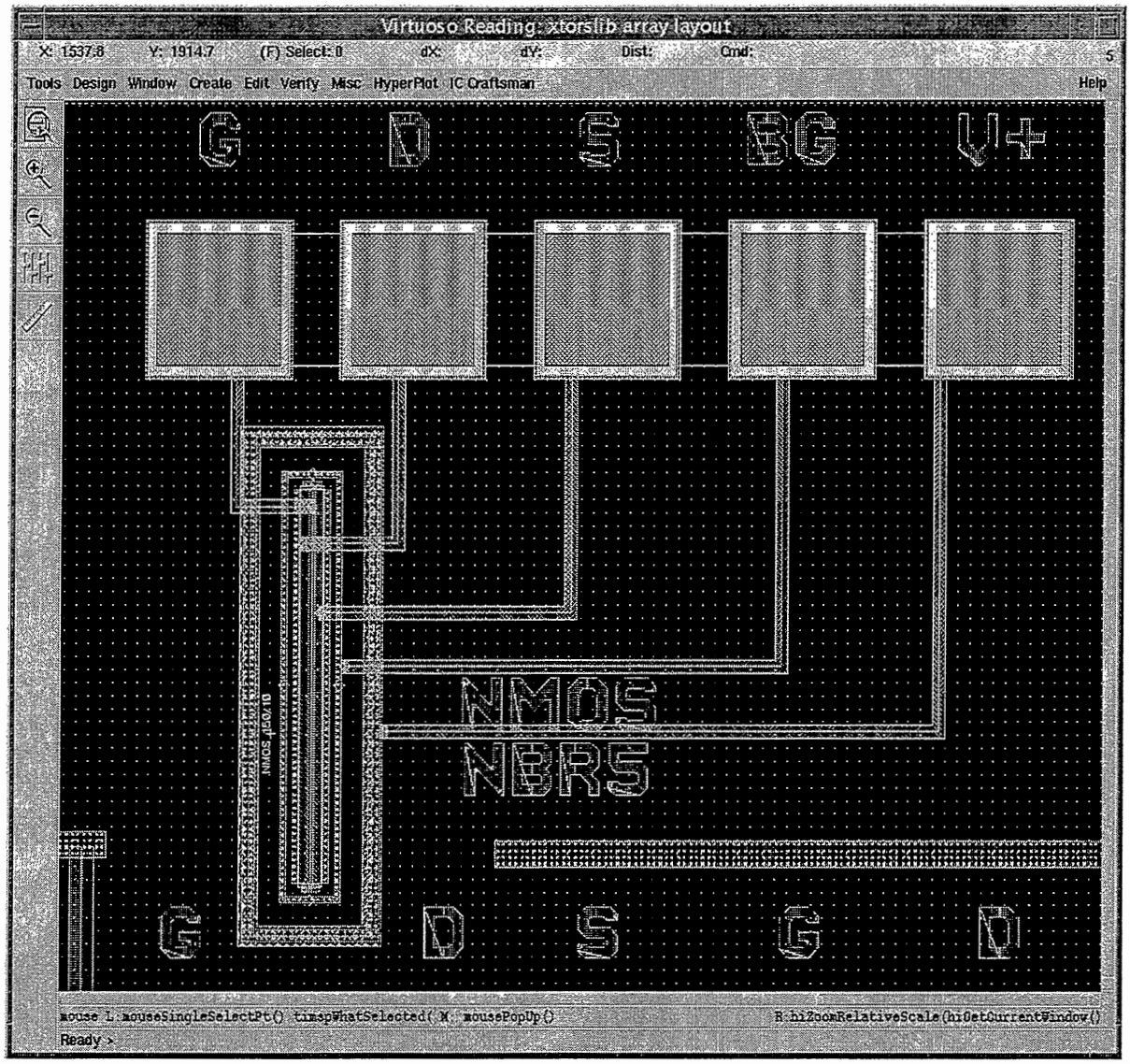


Figure A.6 – Layout of test structure NMOS NBR5 of Table A.1

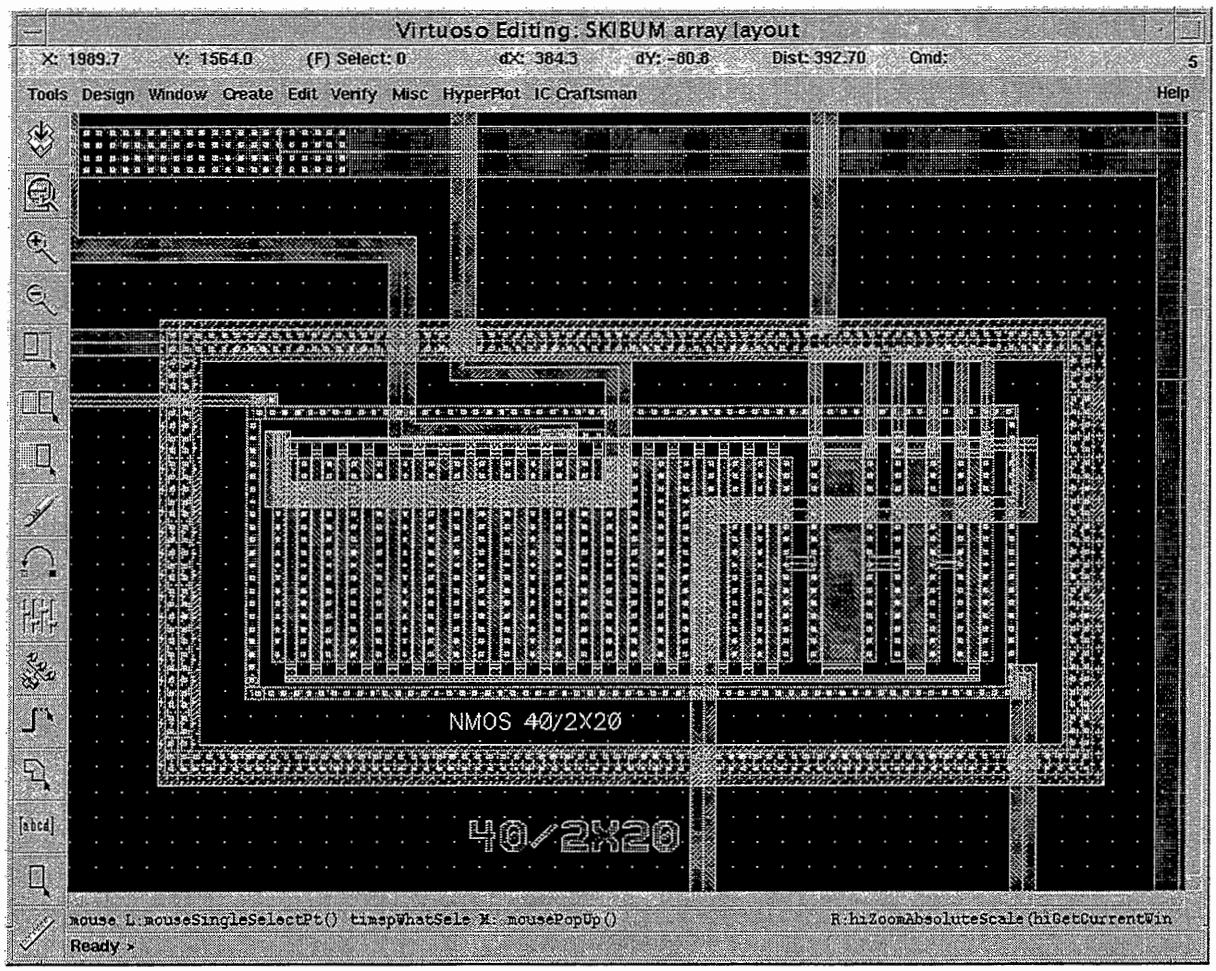


Figure A.7 – Layout of test structure NMOS NBR8 device 40/2x20 of Table A.1

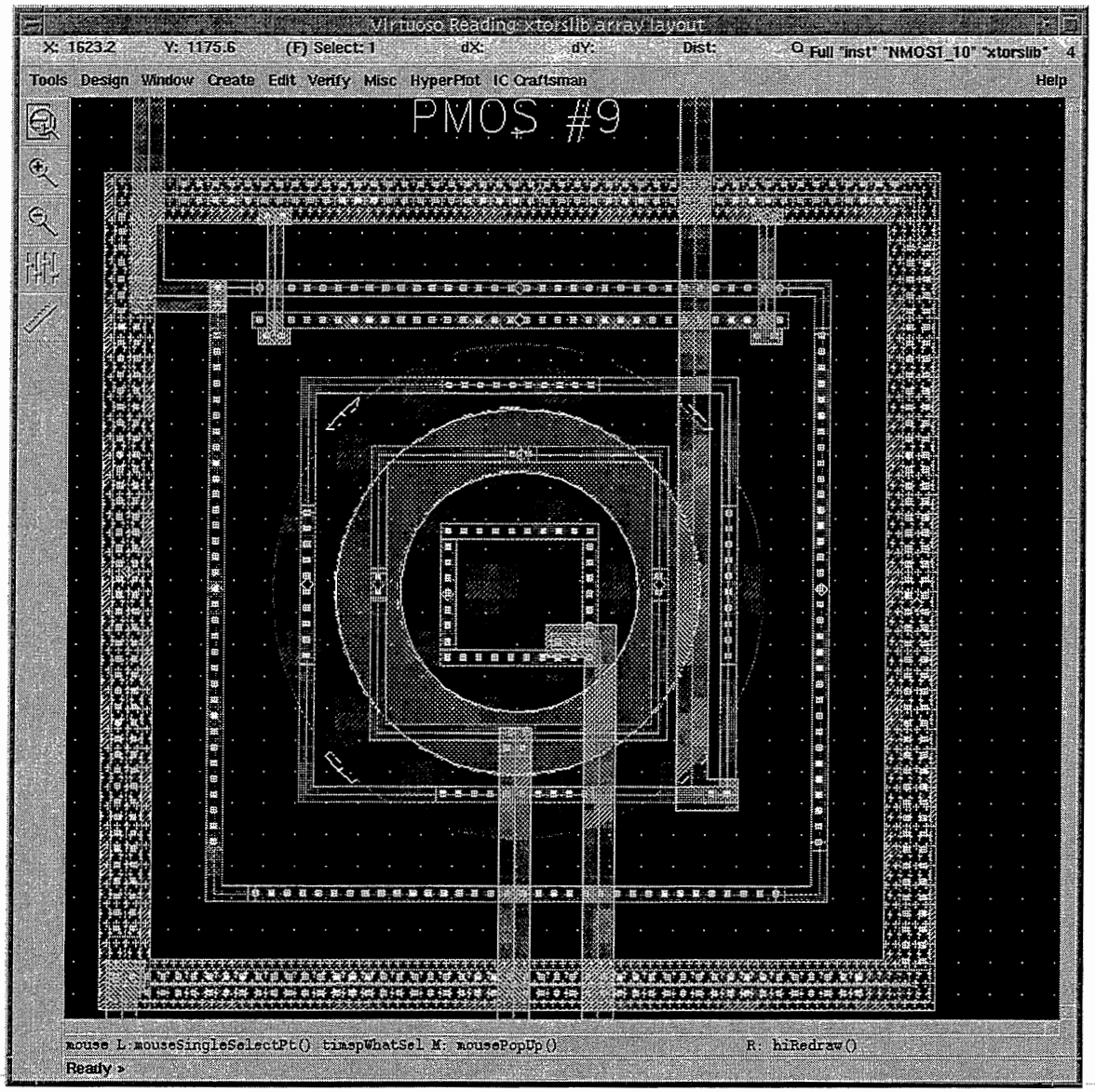


Figure A.8 – Layout of test structure PMOS NBR9 of Table A.1

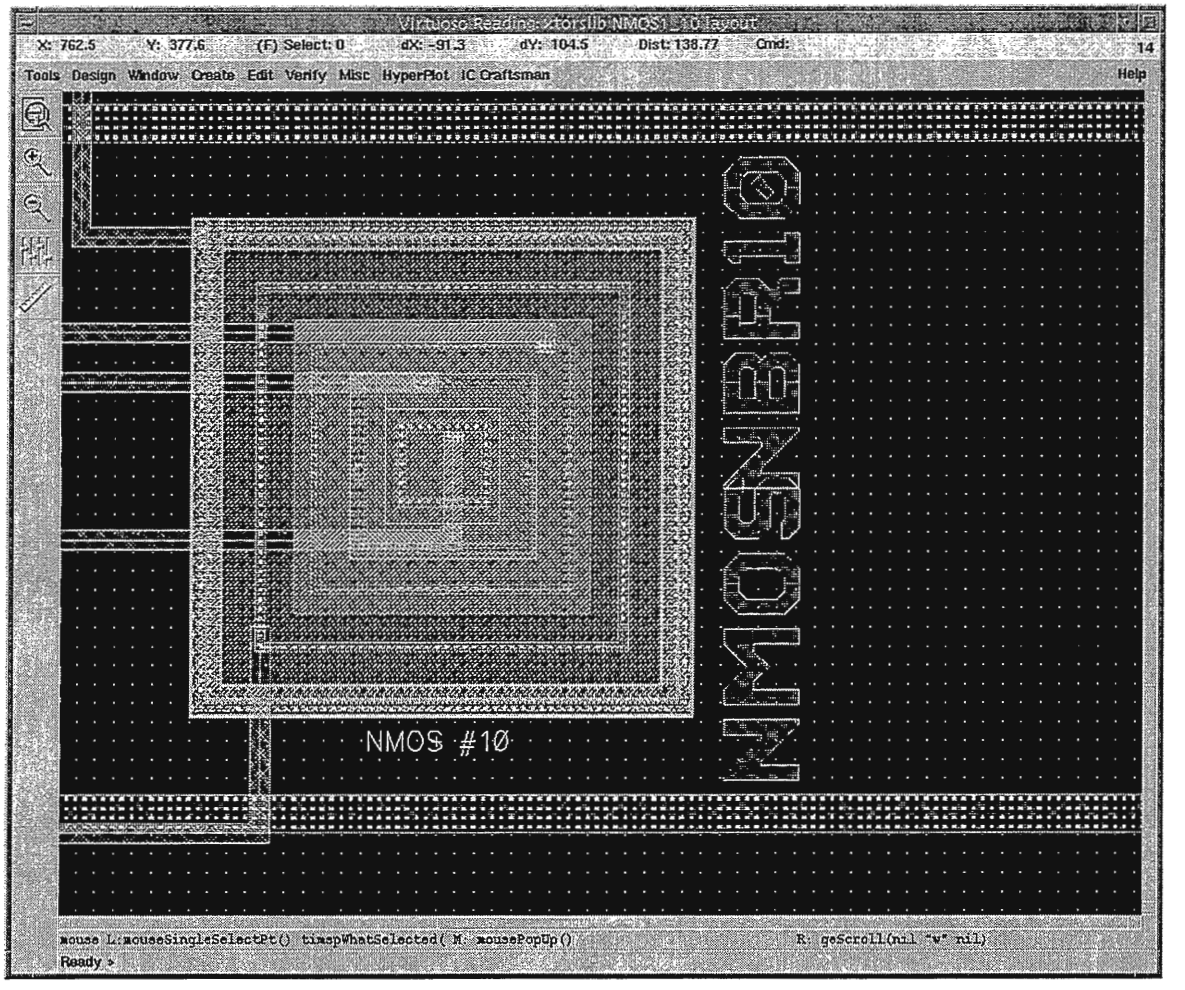


Figure A.9 – Layout of test structure NMOS NBR10 of Table A.1

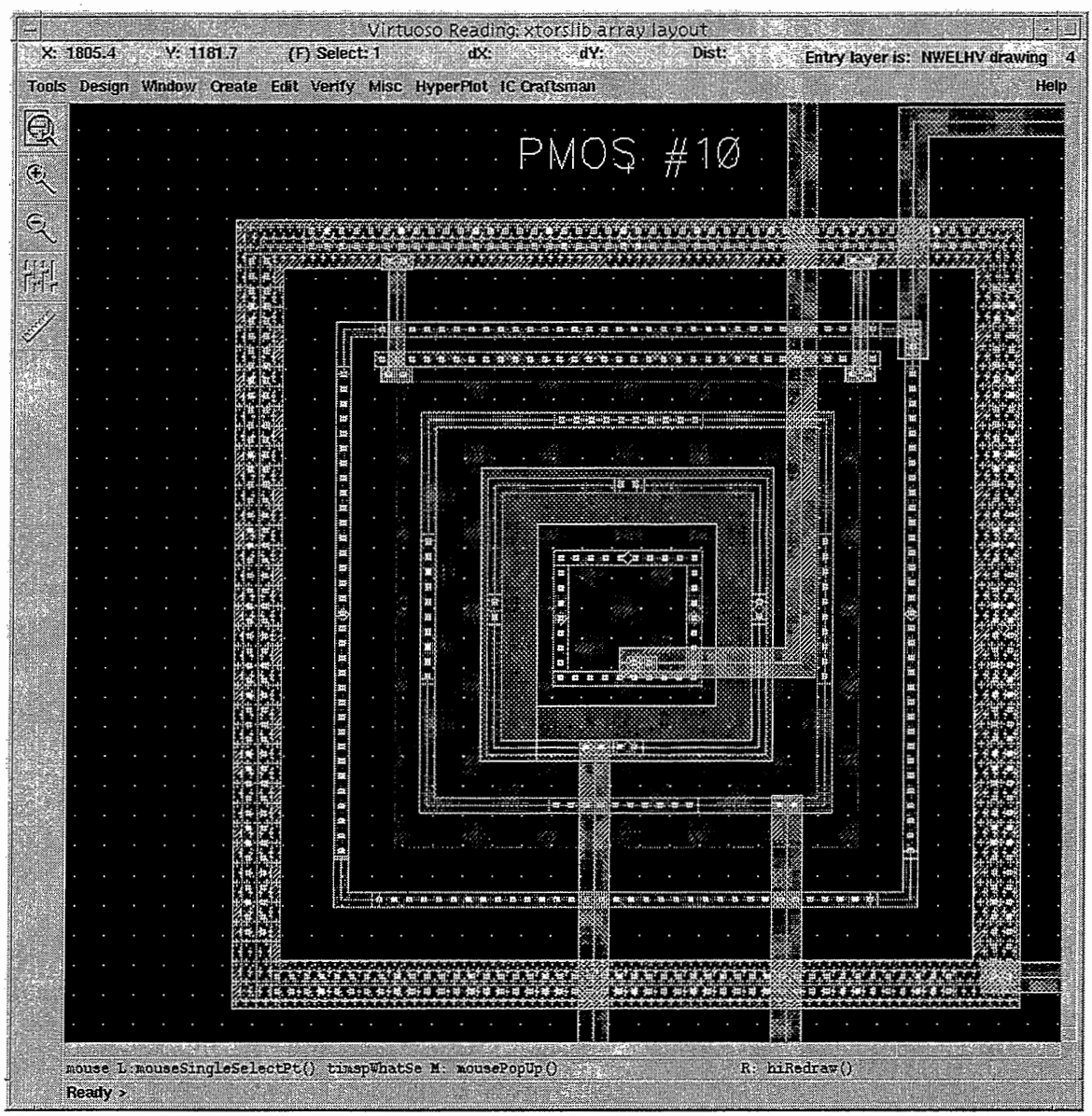


Figure A.10 – Layout of test structure PMOS NBR10 of Table A.1

LBC3S - Lot 9947456 Wafer #7

Data for NMOS

Rectangular - Module NBR1

						With arbitrary slope (slope <> -1)				With slope = -1				TI Values		
						Removing 40 data pts		With original data		Removing 40 data pts		With original data				
						With new weight		With Equal weight		With new weight		With Equal weight				
No.	Die	W/L	Vgs (V)	Vds (V)	Idc (uA)	Kf (Am^2)	RMS Error	Kf_equalwt (Am^2)	RMS Error	Kf (Am^2)	RMS Error	Kf_equalwt (Am^2)	RMS Error	Kf (Am^2)	RMS Error	Comments
1	63	150/10	1.5	4	186.7	6.23E-14	0.40%	7.76E-14	0.98%	9.75E-14	0.52%	1.28E-13	1.00%	1.22E-13	0.69%	**Rectangular**
2	43	150/10	1.5	4	188.3	5.62E-14	0.33%	4.65E-14	0.98%	7.21E-14	0.44%	8.84E-14	1.01%	8.40E-14	0.62%	
3	44	150/10	1.5	4	181.2	5.71E-14	0.35%	5.46E-14	1.00%	8.34E-14	0.47%	1.05E-13	1.03%	9.99E-14	0.7%	
4	45	150/10	1.5	4	181.7	5.63E-14	0.35%	5.27E-14	1.08%	8.96E-14	0.63%	1.29E-13	1.13%	1.22E-13	0.78%	
5	46	150/10	1.5	4	185.3	6.40E-14	0.36%	4.73E-14	1.05%	7.38E-14	0.43%	8.99E-14	1.07%	8.53E-14	0.67%	
6	33	150/10	1.5	4	190.0	7.03E-14	0.35%	5.52E-14	1.04%	8.67E-14	0.44%	1.05E-13	1.07%	9.96E-14	0.69%	
7	34	150/10	1.5	4	189.3	1.52E-13	0.33%	1.27E-13	0.68%	1.82E-13	0.42%	2.17E-13	0.71%	1.18E-13	0.72%	
				Kf mean		**7.40E-14**						**1.23E-13**		**1.04E-13**		
				Kf final		**6.10E-14**	(Ignoring 34)				(Ignoring 34)	**1.08E-13**		**1.08E-13**	(Ignoring 43)	
Circular - Module NBR9																
1	63	150/10	1.5	4	189.2	5.96E-14	0.35%	5.14E-14	1.04%	6.70E-14	0.38%	7.75E-14	1.05%	7.43E-14	0.65%	**Circular**
2	43	150/10	1.5	4	191.0	4.25E-14	0.38%	3.04E-14	1.05%	5.64E-14	0.53%	7.23E-14	1.10%	6.74E-14	0.75%	
3	44	150/10	1.5	4	183.5	5.33E-14	0.36%	4.26E-14	1.03%	6.90E-14	0.44%	8.33E-14	1.06%	7.87E-14	0.71%	
4	45	150/10	1.5	4	185.3	4.72E-14	0.35%	4.49E-14	1.03%	7.82E-14	0.67%	1.16E-13	1.09%	1.09E-13	0.84%	
5	46	150/10	1.5	4	184.9	Bad Data										Good DC but bad AC
5	33	150/10	1.5	4	192.7	1.52E-13	0.33%	1.27E-13	0.68%	1.82E-13	0.42%	2.17E-13	0.71%	8.03E-14	0.82%	
6	34	150/10	1.5	4	191.9	5.78E-14	0.35%	4.83E-14	0.98%	5.90E-14	0.36%	6.04E-14	0.99%	5.77E-14	0.61%	
				Kf mean		**6.87E-14**	(Ignoring 46)				(Ignoring 46)	**1.04E-13**		**7.79E-14**	(Ignoring 46)	
				Kf final		**5.21E-14**	(Ignoring 33,46)				(Ignoring 33,46)	**8.19E-14**		**7.17E-14**	(Ignoring 45,46)	
Concentric - Module NBR10																
1	63	150/10	1.5	4	189.4	6.48E-14	0.38%	4.70E-14	1.13%	7.69E-14	0.47%	9.79E-14	1.16%	9.32E-14	0.81%	**Concentric**
2	43	150/10	1.5	4	189.7	1.11E-12	0.37%	1.26E-12	0.82%	1.08E-12	0.37%	1.06E-12	0.82%	1.03E-12	0.59%	Too high noise curve
3	44	150/10	1.5	4	183.7	6.11E-14	0.36%	5.44E-14	1.17%	8.65E-14	0.52%	1.17E-13	1.20%	1.10E-13	0.91%	
4	45	150/10	1.5	4	185.7	3.07E-14	0.37%	2.68E-14	1.15%	6.07E-14	0.88%	1.03E-13	1.25%	9.50E-14	0.99%	Fitting was not very good
5	46	150/10	1.5	4	189.3	6.18E-14	0.36%	4.54E-14	1.09%	7.05E-14	0.43%	8.56E-14	1.12%	8.10E-14	0.71%	
6	33	150/10	1.5	4	193.0	4.66E-14	0.37%	3.69E-14	1.16%	7.58E-14	0.72%	1.16E-13	1.23%	1.08E-13	0.94%	
7	34	150/10	1.5	1.5	191.7	5.12E-14	0.36%	4.22E-14	1.13%	6.48E-14	0.47%	8.33E-14	1.16%	7.88E-14	0.76%	
				Kf mean		**2.03E-13**						**2.37E-13**		**2.28E-13**		
				Kf final		**5.27E-14**	(Ignoring 43)				(Ignoring 43)	**1.00E-13**		**9.43E-14**	(Ignoring 43)	
Multiple devices in parallel - Module NBR4																
55 devices in parallel - Effective W/L=212.5/10 before width reduction																
1	63	150/10	1.55	4	185.9	9.13E-14	0.37%	8.67E-14	1.04%	1.09E-13	0.39%	1.26E-13	1.04%	1.19E-13	0.72%	
2	43	150/10	1.55	4	186.3	7.79E-14	0.31%	6.58E-14	0.97%	9.19E-14	0.39%	1.10E-13	0.99%	1.05E-13	0.59%	
3	44	150/10	1.55	4	180.1	8.69E-14	0.37%	6.46E-14	1.12%	9.43E-14	0.41%	1.11E-13	1.14%	1.05E-13	0.68%	
4	45	150/10	1.55	4	181.1	7.10E-14	0.33%	5.93E-14	1.08%	1.01E-13	0.49%	1.30E-13	1.12%	1.22E-13	0.71%	
5	46	150/10	1.55	4	186.1	7.50E-14	0.35%	5.89E-14	1.04%	9.34E-14	0.47%	1.19E-13	1.07%	1.12E-13	0.69%	
6	33	150/10	1.55	4	189.8	5.29E-14	1.02%	5.34E-14	1.02%	8.99E-14	0.64%	1.30E-13	1.07%	1.23E-13	0.74%	
7	34	150/10	1.55	4	187.1	6.12E-14	0.31%	5.05E-14	0.95%	7.98E-14	0.48%	1.02E-13	0.99%	9.76E-14	0.64%	
				Kf mean		**7.38E-14**						**1.19E-13**		**1.12E-13**		
				Kf final		**7.72E-14**	(Ignoring 33)				(Ignoring 34)	**1.21E-13**		**1.14E-13**	(Ignoring 34)	

Note:

1. One data point with highest deviation from mean was thrown away from set. Kf final value is considered for calculation.
2. RMS error is always lower with new algorithm and with new weight. Providing equal weight gives higher RMS error as seen from data and fit.

PMOS MEASUREMENTS

LBC3S - Lot 9947456 Wafer #7

Data for PMOS

						With arbitrary slope (slope <> -1)				With slope = -1				TI Values		
						Removing 40 data pts With new weight		With original data With Equal weight		Removing 40 data pts With new weight		With original data With Equal weight				
No.	Die	W/L	Vgs (V)	Vds (V)	Idc (uA)	Kf (Am^2)	RMS Error	Kf_equalwt (Am^2)	RMS Error	Kf (Am^2)	RMS Error	Kf_equalwt (Am^2)	RMS Error	Kf (Am^2)	RMS Error	Comments
Rectangular - Module NBR1																
1	104	150/10	3.5	4	739.4	1.71E-14	0.72%	7.85E-15	1.59%	6.33E-15	0.82%	5.65E-15	1.59%	4.91E-15	1.29%	**Rectangular**
2	44	150/10	3.5	4	762.6	2.23E-14	0.48%	1.28E-14	1.25%	8.67E-15	0.79%	6.51E-15	1.28%	6.13E-15	0.88%	
3	45	150/10	3.5	4	761.9	1.50E-14	0.46%	9.04E-15	1.19%	6.04E-15	0.69%	4.71E-15	1.21%	4.50E-15	0.77%	
4	46	150/10	3.5	4	756.1	2.04E-14	0.59%	9.54E-15	1.27%	5.93E-15	0.57%	5.43E-15	1.29%	5.05E-15	0.84%	
5	33	150/10	3.5	4	748.7	3.18E-14	0.52%	2.00E-14	1.21%	1.10E-14	0.86%	7.93E-15	1.26%	7.38E-15	0.94%	
6	34	150/10	3.5	4	755.1	2.07E-14	0.43%	1.34E-14	1.15%	8.47E-15	0.63%	6.89E-15	1.18%	6.47E-15	0.74%	
7	76	150/10	3.5	4	774.5	2.01E-14	0.47%	1.33E-14	1.26%	7.99E-15	0.71%	6.57E-15	1.29%	5.91E-15	0.8%	
8	66	150/10	3.5	4	762	1.74E-14	0.65%	8.69E-15	1.29%	5.21E-15	0.80%	4.29E-15	1.32%	3.74E-15	0.9%	
				Kf mean		**2.06E-14**						**6.00E-15**		**5.51E-15**		
				Kf final		**1.90E-14**	(Ignoring 33)				(Ignoring 33)	**5.72E-15**		**5.24E-15**	(Ignoring 33)	
Circular - Module NBR9																
1	104	150/10	3.5	4	734.7	1.48E-14	0.44%	9.08E-15	1.15%	8.68E-15	0.39%	8.48E-15	1.15%	7.97E-15	0.58%	**Circular**
2	44	150/10	3.5	4	759.1	1.99E-14	0.52%	9.57E-15	1.26%	4.83E-15	0.70%	3.88E-15	1.30%	3.69E-15	0.88%	
3	45	150/10	3.5	4	759.4	1.66E-14	0.58%	7.35E-15	1.24%	5.13E-15	0.54%	4.55E-15	1.26%	4.31E-15	0.77%	
4	46	150/10	3.5	4	748.8	1.72E-12	1.02%	3.63E-13	1.31%	2.11E-14	1.70%	1.10E-14	1.85%	1.20E-14	2.45%	
5	33	150/10	3.5	4	747.4	1.71E-14	0.44%	1.03E-14	1.18%	5.60E-15	0.69%	4.41E-15	1.22%	4.26E-15	0.88%	
5	34	150/10	3.5	4	750.7	1.26E-14	0.52%	6.75E-15	1.27%	5.51E-15	0.45%	5.33E-15	1.27%	5.08E-15	0.77%	
6	76	150/10	3.5	4	759	1.64E-14	0.46%	9.88E-15	1.17%	6.79E-15	0.52%	5.91E-15	1.19%	5.68E-15	0.71%	
7	66	150/10	3.5	4	756.9	4.14E-14	1.25%	2.21E-14	1.20%	8.05E-15	0.99%	5.41E-15	1.31%	5.34E-15	1.11%	
				Kf mean		**2.33E-13**						**6.12E-15**		**6.04E-15**		
				Kf final		**1.98E-14**	(Ignoring 46)				(Ignoring 46)	**5.43E-15**		**5.19E-15**	(Ignoring 46)	
Concentric - Module NBR10																
1	104	150/10	3.5	4	728.3	1.61E-14	0.42%	1.02E-14	1.19%	5.94E-15	0.58%	5.05E-15	1.21%	4.87E-15	0.77%	**Concentric**
2	44	150/10	3.5	4	752.9	1.31E-14	0.49%	7.23E-15	1.18%	6.06E-15	0.44%	5.73E-15	1.18%	5.43E-15	0.65%	
3	45	150/10	3.5	4	751.3	4.59E-14	0.40%	3.02E-14	1.02%	2.33E-14	0.58%	1.86E-14	1.04%	1.80E-14	0.66%	
4	46	150/10	3.5	4	745.2	1.78E-14	0.49%	9.08E-15	1.24%	6.01E-15	0.67%	4.71E-15	1.27%	4.49E-15	0.78%	
5	33	150/10	3.5	4	742.8	1.82E-14	0.59%	8.53E-15	1.26%	5.45E-15	0.73%	4.50E-15	1.28%	4.16E-15	0.95%	
6	34	150/10	3.5	4	744.8	1.46E-14	1.20%	8.97E-15	1.17%	7.99E-15	0.42%	7.58E-15	1.17%	7.20E-15	0.67%	
7	76	150/10	3.5	4	753.9	1.68E-14	0.57%	7.63E-15	1.26%	4.49E-15	0.64%	3.72E-15	1.29%	3.53E-15	0.83%	
8	66	150/10	3.5	4	749.4	2.09E-14	0.41%	1.36E-14	1.19%	6.97E-15	0.79%	5.08E-15	1.25%	4.90E-15	0.84%	
				Kf mean		**2.04E-14**						**6.87E-15**		**6.57E-15**		
				Kf final		**1.68E-14**	(Ignoring 45)				(Ignoring 45)	**5.19E-15**		**4.94E-15**	(Ignoring 45)	
Multiple devices in parallel - Module NBR4																
55 devices in parallel - Effective W/L=212.5/10 before width reduction																
1	74	150/10	3.5	4	756.5	1.59E-14	0.48%	8.93E-15	1.21%	6.38E-15	0.49%	5.88E-15	1.22%	5.64E-15	0.76%	
2	104	150/10	3.5	4	735.9	3.74E-14	0.37%	2.92E-14	1.03%	2.68E-14	0.44%	2.46E-14	1.03%	2.34E-14	0.61%	
3	44	150/10	3.5	4	760.2	1.93E-14	0.61%	8.77E-15	1.17%	6.53E-15	0.62%	5.44E-15	1.18%	5.16E-15	0.81%	
4	45	150/10	3.5	4	751.6	1.79E-14	0.48%	9.92E-15	1.20%	6.17E-15	0.64%	5.02E-15	1.22%	4.81E-15	0.79%	
5	46	150/10	3.5	4	749.2	1.91E-14	0.47%	1.08E-14	1.23%	6.42E-15	0.72%	4.87E-15	1.26%	4.68E-15	0.81%	
6	33	150/10	3.5	4	741.3	1.25E-14	0.48%	6.90E-15	1.24%	5.11E-15	0.47%	4.72E-15	1.24%	4.50E-15	0.74%	
7	34	150/10	3.5	4	745.2	1.39E-14	0.39%	1.00E-14	1.20%	7.13E-15	0.47%	6.47E-15	1.21%	6.12E-15	0.71%	
8	76	150/10	3.5	4	760.9	1.94E-14	0.56%	9.03E-15	1.14%	7.99E-15	0.43%	7.67E-15	1.14%	7.29E-15	0.68%	
9	66	150/10	3.5	4	731	**BAD DATA**										
10	56	150/10	3.5	4	644	**BAD DATA**										
				Kf mean		**1.94E-14**						**8.08E-15**		**7.70E-15**		
				Kf final		**1.68E-14**	(Ignoring 104)				(Ignoring 104)	**5.72E-15**		**5.46E-15**	(Ignoring 104)	

Note:

1. One data point with highest deviation from mean was thrown away from set. Kf final value is considered for calculation.
2. RMS error is always lower with new algorithm and with new weight. Providing equal weight gives higher RMS error as seen from data and fit.

APPENDIX C

MATLAB CODE FOR DATA EXTRACTION

DATAPROCESS.M

```
%This program finds out all the cmosnoise.data files from current path and will process the data with
%new algorithm. Kf will be extracted with both arbitrary slope and fixed slope.

currentdir = 'c:\winnt\profiles\dagli\desktop\lbc3s_vgs\9947456\07';
cd (currentdir);
m=0;
homedir = dir; %base directory contains all die names

for i=1:length(homedir)
  if getfield(homedir(i),'isdir')
                                          %to make sure for . and .. dirs
    if   (strcmp(homedir(i).name,'.') | strcmp(homedir(i).name,'..'))

    else
        die=homedir(i).name;
        currentdiepath=[currentdir,'\',die];
        cd(currentdiepath);
        tempmodules = dir;
        for j=1:length(tempmodules) %look for modules inside die
            if getfield(tempmodules(j),'isdir')
                if      (strcmp(tempmodules(j).name,'.') | strcmp(tempmodules(j).name,'..'))
                                %to make sure for . and .. dirs
                else
                        module = tempmodules(j).name;
                        currentmodulepath = [currentdiepath,'\',module];
                        cd(currentmodulepath);
                        tempdevices = dir;
                        for k=1:length(tempdevices) %look for devices inside a module
                            if getfield(tempdevices(k),'isdir')
                                if(strcmp(tempdevices(k).name,'.') | strcmp(tempdevices(k).name,'..'))
                                                %to make sure for . and .. dirs
                                else
                                    device = tempdevices(k).name;
                                    currentdevicepath= [currentmodulepath,'\',device];
                                    cd(currentdevicepath);
                                    tempdata = dir;
                                    datafiles = strvcat(tempdata(:,1).name);
                                    findcmos = strmatch('cmosnoise.data',datafiles);
```

```
                                    if (length(findcmos) ~= 0)
                                        m=m+1;
                                        [Kf(m),Kf0(m),Kf_equalwt(m)]=
                                                kfextract_auto_arbslope(currentdevicepath);
                                        [Kf_1(m),Kf0_1(m),Kf_equalwt_1(m)]=
                                                kfextract_auto_fixedslope(currentdevicepath);
                                    end
                                end
                            end
                        end
                    end
                end
            end
        end
    end
end
disp('Total # of files processed = ');disp(m); %Total # of files processed successfully and Kf extracted
```

KFEXTRACT_AUTO_ARBSLOPE.M

```
%This function find Kf(flicker noise co-efficient) from given data files cmosnoise.data and
%device.attr It uses the weighted least square algorithm using matrix calculations. Slope of fitted
%line is arbitrary and doesnt have to be one This program is called from another program and
%hence it cannot be run independently

function [Kf,Kf0,Kf_equalwt] = kfextract_auto(cmosdirectory)

close all;
homedir = cmosdirectory;

fid = fopen('cmosnoise.data','r');

for i = 1:12
    line = fgetl(fid);
end
format short e;
[A] = fscanf(fid, '%f', [10,801]);
fclose(fid);

b=A'; %b is 801x10 matrix obtained from cmosnoise.data
freq = b(:,1);
FNP = b(:,9);  %original data - flicker noise power
```

```
W =1 ./freq; %weight proportional to 1/f
W0=1; %equal weight - any constant

%linear regression with equal weight - (alternatively g02caf function can be used as well)
[COEF0,FITS0,RES0] = weightedlsq(FNP,freq,W0);
FNPNEW0 = 10.^FITS0; %fitted FNP with equal weight
%[result] = g02caf(log10(freq),log10(FNP)); %linear regression without weight
%result(6) %slope
%result(7) %intercept
% weighted linear regression
[COEF,FITS,RES] = weightedlsq(FNP,freq,W);
FNPNEW = 10.^FITS; %fitted FNP

loglog(freq,FNP,'k',freq,FNPNEW0,'m',freq,FNPNEW,'k');
hold on;
% black - original, black - 1st weighted fit , magenta - fit with equal %weight
%try to remove top 20 points from sorted residuals and plot again

[FNPremoved, freqremoved] = Remove20Data(freq,FNP,FITS,RES);
loglog(freqremoved,FNPremoved,'g');

%hold on;
W1 = 1 ./freqremoved; %weight proportional to 1/f

[COEF1,FITS1,RES1] = weightedlsq(FNPremoved,freqremoved,W1);
FNPNEW1 = 10.^FITS1;

loglog(freqremoved,FNPNEW1,'g'); %after removing top 20, fitted FNP
%hold on;
[FNPremoved1, freqremoved1] = Remove20Data(freqremoved,FNPremoved,FITS1,RES1);
%Remove next 20

loglog(freqremoved1,FNPremoved1,'r');
%hold on;

W2 = 1 ./freqremoved1; %weight proportional to 1/f

[COEF2,FITS2,RES2] = weightedlsq(FNPremoved1,freqremoved1,W2);
FNPNEW2 = 10.^FITS2;
intercept = 10 .^ COEF2(1);
intercept_original = 10 .^ COEF(1);
intercept_old = 10 .^ COEF0(1);
slope = COEF2(2);

axis tight;
```

```
xlabel('Frequency (Log)');
ylabel('Current spectral noise density SI (Log)');
title('Fitting with arbitrary slope');
ylimit = ylim;
text(2,ylimit(2)/4,{'Black -  Original data','Pink   -  Fit with equal weight on original data','Green -
After removing 20 points','Red    -  After removing 40 points'});

loglog(freqremoved1,FNPNEW2,'r');

%finding RMS error
RESsq = RES2 .^ 2;
RESsq_original = RES .^ 2; %For original data without removing any data points but with new
%weight
RESsq_equalwt = RES0 .^ 2;

errsq = sum(RESsq); %sum of square of residuals
errsq_original = sum(RESsq_original);
errsq_equalwt = sum(RESsq_equalwt);

RMSerr = sqrt(errsq) ./length(RESsq) * 100; %percentage rms error
RMSerr0 = sqrt(errsq_original) ./length(RESsq_original) * 100;
RMSerr_equalwt = sqrt(errsq_equalwt) ./length(RESsq_equalwt) * 100

fname = 'device.attr';

len = loadlength(homedir, fname); %returns the length of device in microns
Ids = abs(b(1,5,1)); % Operating point drain current

Kf = intercept*len^2/Ids; %Flicker noise co-efficient
Kf0 = intercept_original*len^2/Ids;
Kf_equalwt = intercept_old*len^2/Ids %with equal weight as TI

%Writing the summary report in performance.txt file in the same path as cmosnoise.data file
ptr = fopen([homedir,'\','Kfreport_arb_slope.txt'],'wt');
fprintf(ptr,['Slope of final fitted line = ', num2str(slope)]);
fprintf(ptr,['\nIntercept of final fitted line = ',num2str(intercept)]);
fprintf(ptr,['\nFlicker Noise Co-efficient Kf = ',num2str(Kf)]);
fprintf(ptr,['\nRMS Error = ', num2str(RMSerr), '%%']);

fprintf(ptr,['\nFlicker Noise Co-efficient Kf0 (with original data and new weight) = ',num2str(Kf0)]);
fprintf(ptr,['\nRMS Error (For Kf0) = ', num2str(RMSerr0), '%%']);

fprintf(ptr,['\nFlicker Noise Co-efficient Kf_equalwt (with original data and equal weight) =
',num2str(Kf_equalwt)]);
fprintf(ptr,['\nRMS Error (For Kf_equalwt) = ', num2str(RMSerr_equalwt), '%%']);
```

```
fclose(ptr);
fit_arbslope = [homedir,'\','fit_arbslope.ps']
print -dpsc fit_arbslope;
```

WEIGHTEDLSQ.M

```
%This function performs weighted least square fit and returns regression  coefficients,residuals and
%fitted values

function [COEF,FITS,RES] = weightedlsq(Y,X,W);

%     Y  - Response variable
%     X  - Predictor variables
%     W  - Weights
%
%     Returns:
%
%     COEF - Coefficients for weighted least squares
%        COEF(1) - intercept
%     COEF(2) - slope
%     FITS - Fitted values
%     RES  - Residuals

X = log10(abs(X))+1e-100; %1e-100 added if data=0
Y = log10(abs(Y))+1e-100; % original data

n = length(Y);
X = [ones(n,1) X];
W = diag(W);

COEF = inv(X'*W*X)*X'*W*Y;
FITS = X*COEF;
RES  = Y-FITS;
```

REMOVE20DATA.M

```
%This funciton removes the top 20 data points which have highest errors-residues
function [FNPremoved, freqremoved] = Remove20Data(freq,FNP,FITS,RES)

original = [freq FNP FITS abs(RES)];
corrected = sortrows(original,4); % sorting according error values(residuals)
L = length(original)-20;
removed = corrected(1:L,:); % just storing freq and corresponding FNP - still sorted according to
%residuals
```

```
New = sortrows(removed,1); %sorting according to frequency

FNPremoved = New(:,2); %corresponding top 20 residuals removed for original FNP
freqremoved = New(1:L,1);
```

LOADLENGTH.M

```
% Find out the length of device from device.attr file
function [len] = loadlength(fpath,fname)

fid=fopen([fpath,'\',fname],'r');

if fid==-1
  error(['Unable to open file: ', fpath, '\', fname]);
end

for i = 1:2
    line = fgetl(fid);
end
format short e;
fseek(fid,16,0);
len = fscanf(fid, '%4d');
fclose(fid);
```

KFEXTRACT_AUTO_FIXEDSLOPE.M

```
%This function find Kf(flicker noise co-efficient) from given data files cmosnoise.data and
% device.attr
%It uses the weighted least square algorithm using formulas for regression co-efficients
function [Kf,Kf0,Kf_equalwt] = kfextract_auto(cmosdirectory)

close all;
homedir = cmosdirectory;

fid = fopen('cmosnoise.data','r');

for i = 1:12
    line = fgetl(fid);
end
format short e;
[A] = fscanf(fid, '%f', [10,801]);
fclose(fid);

b=A'; %b is 801x10 matrix obtained from cmosnoise.data
freq = b(:,1);
FNP = b(:,9);  %original data - flicker noise power
```

```
W =1 ./freq; %weight proportional to 1/f
W0= ones([801,1]); %equal weight - any constant

%linear regression with equal weight - (alternativelyl g02caf function can be used as well
[COEF0,FITS0,RES0] = weightedlsq_calc(FNP,freq,W0);
FNPNEW0 = 10.^FITS0; %fitted FNP with equal weight
%[result] = g02caf(log10(freq),log10(FNP)); %linear regression without weight
%result(6) %slope
%result(7) %intercept

% weighted linear regression
[COEF,FITS,RES] = weightedlsq_calc(FNP,freq,W);
FNPNEW = 10.^FITS; %fitted FNP

loglog(freq,FNP,'k',freq,FNPNEW0,'m',freq,FNPNEW,'k');
hold on;
% black - original, black - 1st weighted fit , magneta - fit with equal weight
%try to remove top 20 points from sorted residuals and plot again

[FNPremoved, freqremoved] = Remove20Data(freq,FNP,FITS,RES);
loglog(freqremoved,FNPremoved,'g');

%hold on;
W1 = 1 ./freqremoved; %weight proportional to 1/f

[COEF1,FITS1,RES1] = weightedlsq_calc(FNPremoved,freqremoved,W1);
FNPNEW1 = 10.^FITS1;

loglog(freqremoved,FNPNEW1,'g'); %after removing top 20, fitted FNP
%hold on;
[FNPremoved1, freqremoved1] = Remove20Data(freqremoved,FNPremoved,FITS1,RES1);
%Remove next 20

loglog(freqremoved1,FNPremoved1,'r');
%hold on;

W2 = 1 ./freqremoved1; %weight proportional to 1/f

[COEF2,FITS2,RES2] = weightedlsq_calc(FNPremoved1,freqremoved1,W2);
FNPNEW2 = 10.^FITS2;
intercept = 10 .^ COEF2(1);
intercept_original = 10 .^ COEF(1);7
intercept_old = 10 .^ COEF0(1);
slope = COEF2(2);
```

```
axis tight;
xlabel('Frequency (Log)');
ylabel('Current spectral noise density SI (Log)');
title('Fitting with fixed slope = -1');
ylimit = ylim;
text(2,ylimit(2)/4,{'Black -  Original data','Pink   -  Fit with equal weight on original data','Green -
After removing 20 points','Red    -  After removing 40 points'});

loglog(freqremoved1,FNPNEW2,'r');

%finding RMS error
RESsq = RES2 .^ 2;
RESsq_original = RES .^ 2; % original data without removing any data points but with new weight
RESsq_equalwt = RES0 .^ 2;

errsq = sum(RESsq); %sum of square of residuals
errsq_original = sum(RESsq_original);
errsq_equalwt = sum(RESsq_equalwt);

RMSerr = sqrt(errsq) ./length(RESsq) * 100 %percentage rms error
RMSerr0 = sqrt(errsq_original) ./length(RESsq_original) * 100
RMSerr_equalwt = sqrt(errsq_equalwt) ./length(RESsq_equalwt) * 100
fname = 'device.attr';

len = loadlength(homedir, fname); %returns the length of device in microns
Ids = abs(b(1,5,1)) % Operating point drain current

Kf = intercept*len^2/Ids %Flicker noise co-efficient
Kf0 = intercept_original*len^2/Ids
Kf_equalwt = intercept_old*len^2/Ids %with equal weight as TI

%Writing the summary report in performance.txt file in the same path as cmosnoise.data file
ptr = fopen([homedir,'\','kfreport_fixed_slope.txt'],'wt');
fprintf(ptr,['Slope of final fitted line = ', num2str(slope)]);
fprintf(ptr,['\nIntercept of final fitted line = ',num2str(intercept)]);
fprintf(ptr,['\nFlicker Noise Co-efficient Kf = ',num2str(Kf)]);
fprintf(ptr,['\nRMS Error = ', num2str(RMSerr), '%%']);

fprintf(ptr,['\nFlicker Noise Co-efficient Kf0 (with original data and new weight) = ',num2str(Kf0)]);
fprintf(ptr,['\nRMS Error (For Kf0) = ', num2str(RMSerr0), '%%']);

fprintf(ptr,['\nFlicker Noise Co-efficient Kf_equalwt (with original data and equal weight) =
',num2str(Kf_equalwt)]);
fprintf(ptr,['\nRMS Error (For Kf_equalwt) = ', num2str(RMSerr_equalwt), '%%']);
fclose(ptr);
```

```
fit_fixedslope = [homedir,'\','fit_fixedslope.ps']
print -dpsc fit_fixedslope;
%print -dpsc c:\winnt\profiles\dagli\desktop\dataprocess\fit.ps;
```

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